

## COMPUTING DEVICE

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### Abstract

A novel computing device capable of performing flexible information processing analogous to that of living things, such as learning, adaption, and self-multiplication, which are essential to implement advanced information processing of the future. The device comprises a plurality of first and second input terminals, and a plurality of operational units which execute a given operation of data signals to be inputted into the first input terminals, and each have at least one terminal for outputting the result of the operation. The output signal from one of the output terminals or the result of a given operational

processing of this output signal is inputted into at least one of the second input terminals. 

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## Description

### Technical Field

The present invention relates to data processing technology, and in particular, relates to a computing device which makes flexible data processing possible.

### Background Art

Conventionally, the central CPU of computers which conducted data processing technologies comprised semiconductor LSI, and this is termed "hardware". The reason for this is that once the CPU has been constructed, the structure thereof cannot be changed, and it is thus an inflexible structure. Computers can only execute a variety of functions by executing operations in order in the circuits in which these functions are fixed by means of programming. However, in order to realize the high level data processing of the future, it will be necessary to provide data processing such as that conducted by living things, such as learning, adaptation, and self-multiplication such as that performed by human beings; presently, no such computers exist.

There have been a number of attempts to realize flexible data processing by means of software technologies; however, the current state is such that such efforts have met with little success. The reason for this is that hardware, which is inflexible, is used as the base, and even if this is realized in an

imitative manner, the burden on the software becomes excessively large, and an enormous amount of time is required even if a supercomputer is employed, so that it is impossible to construct a system which is capable of rapid response.

The so-called "neural networks", which imitate the data processing of the human brain, have been researched and developed as one powerful method for solving such problems; however, these are still far from practical application. The reason for this is that the data processing of the human brain itself is poorly understood, so that the network imitates an extremely primitive structure, and there is no concrete theoretical construction method.

With respect to this, a high performance transistor, termed a "neuron MOS transistor" (inventors: Tadashi Shibata, Tadahiro Ohmi, Japanese Patent Application, Provisional Publication, No. Hei 3-6679) has been invented, and a soft-hardware circuit to which this is applied (inventors: Tadashi Shibata, Tadahiro Ohmi, Japanese Patent Application No. Hei 3-83135) has been invented. In particular, this soft-hardware circuit possesses extremely flexible hardware, the computing functions of which can be freely altered in response to an external signal. When such flexible hardware is employed as the base, there is a possibility of realizing the flexible data processing which was discussed in the opening paragraph; however, a method for this realization has not as yet been made clear.

The present invention has as an object thereof to provide a novel computing device which is capable of forming flexible information processing analogous to that of living things, such as learning, adaptation, and self-multiplication, which are essential to the realization of advanced information processing of the future.

#### Brief Description of the Diagrams

Fig. 1 is a block diagram explaining the first embodiment.

Fig. 2 is a conceptual diagram of a 4-input N-channel nu MOS transistor.

Fig. 3 is a circuit diagram showing an example of a neuron circuit.

Fig. 4 is an FPD explaining the operation of a neuron circuit.

Fig. 5 is a circuit diagram showing a diagram of a neuron circuit.

Fig. 6 is a circuit diagram showing a diagram of SHL.

Fig. 7 is FPD of a nu MOS inverter 302.

Fig. 8 is a circuit diagram of SD number full adder explaining a second embodiment.

Fig. 9 is a circuit diagram showing an SD number full adder explaining the second embodiment.

Fig. 10 shows the FPD of a nu MOS inverter.

Fig. 11 shows the FPD of a nu MOS inverter.

Fig. 12 shows the FPD of a nu MOS inverter.

Fig. 13 shows the FPD of a nu MOS inverter.

Fig. 14 shows a circuit which conducts the addition of binary SD numbers.

Fig. 15 is a block diagram for explaining a third embodiment.

Fig. 16 is a block diagram for explaining a third embodiment.

Fig. 17 is a block diagram showing a fourth embodiment.

Fig. 18 is a circuit diagram showing another example of the present invention.

## (Description of the References)

101a, 101b, 101c, 101d logical computing units,  
 102a, 102b input terminals,  
 103 output terminal  
 104a, 104b, 104c, 104d control signal input terminals,  
 105b, 105c control input terminals,  
 201 substrate,  
 202, 203 source and drain  
 204 gate insulating film (for example, SiO<sub>2</sub> film),  
 205 channel region,  
 206 floating gate electrode,  
 207 insulating film,  
 208a, 208b, 208c, 208d control gate electrodes,  
 210 N-channel nu MOS,  
 211 P-channel nu MOS,  
 212 nu MOS inverter,  
 213 standard inverter,  
 214 floating gate,  
 301 D/A converter,  
 302, 303, 304, 305, 306 nu MOS inverters.

## Disclosure of the Invention

The computing device in accordance with the present invention is provided with a plurality of first input terminals and a plurality of second input terminals, and a plurality of operational units which execute given operational processing with respect to data signals which are inputted into the first input terminal, by means of control signals inputted into the second input terminals, and which each have at least one output terminal for outputting the results of the operation; characterized in that the output signal from one of the output terminals or the result of a given operational processing of this output signal is inputted to at least one of the second input terminals.

## Best Mode for Carrying Out the Invention

Hereinbelow, embodiments of the present invention will be explained using the diagrams.

## (Embodiment 1)

Fig. 1(a) is a block diagram showing a first embodiment of the invention. This circuit conducts the following operational processing with respect to 4 digital input signals X1 SIMILAR X4. If  $X1 = X3 = 1$ , then when  $X2 = 0$  or  $X4 = 1$ , "1" is outputted, and in all other cases, that is to say, in cases in which one or the other of  $X1$  or  $X3$  is not equal to 1, a value of "1" is outputted only when  $X1$  NOTEQUAL  $X2$  and  $X3 = X4$ .

The present circuit is comprised by connecting four logical operational units A, B, C, and D (101a SIMILAR 101d) to one another by means of wiring. Each operational unit is provided with two input terminals (102a, 102b, and the like), one output terminal 103, and four control signal input terminals (104a, 104b, 104c, 104d, and the like), and the operational functions are stipulated by means of a signal having a value of 0 or 1 which is inputted into the control input terminals. A value of 0 indicates that 0V and a value of 1 indicates that the power source voltage VDD (5V), respectively, are applied to the input terminals. In such a circuit, soft-hardware logical circuits (Japanese Patent Application No. Hei 3-83135) using, for example, neuron MOS transistors (Japanese Patent Application, Provisional Publication, No. Hei 3-6679) may be employed. The neuron MOS transistor and the soft-hardware logical circuit are separately explained.

The blocks A, B, and C become, respectively, NAND circuits, XOR circuits, and XNOR circuits, in response to the input signals into the control input terminals (104a SIMILAR 104d) which are shown in the figure. In the case of block D, the two control input terminals 105b and 105c have the outputs of block A (NAND circuit) inputted thereinto rather than fixed signals, so that if the output 103 has a value of 0, this block becomes an OR circuit, while if the value is 1, the block becomes an AND circuit. These

relationships are depicted in a simplified form in Fig. 1(b).

The portion corresponding to block D has functions which differ depending on the results of the NAND operation of X1 and X3.

As shown above, in the present embodiment, the circuit executes a flexible operational function by means of altering the functions of a portion of a circuit or altering the functions of the entirety of the circuit by means of the operational results.

In the foregoing, an extremely simplified case was shown, so that the importance of this novel flexible function may not be clear; however, this will be discussed in detail in the second embodiment, after the explanation of the neuron MOS transistor and the soft-hardware logical circuit using, respectively, Figs. 2 SIMILAR 7.

First, the structure and operational principle of the neuron MOS transistor (hereinbelow abbreviated to "nu MOS") will be explained. Fig. 2 shows an example of the cross sectional structure of a 4-input N-channel nu MOS transistor; reference 201 indicates, for example, a P-type silicon substrate, references 202 and 203 indicate a source and drain formed from N diffusion layers, reference 204 indicates a gate insulating film (for example, SiO<sub>2</sub> film) which is provided on channel region 205 between the source and the drain, reference 206 indicates a floating gate electrode which is electrically insulated and is in a potentially floating state; reference 207 indicates an insulating film comprising, for example, SiO<sub>2</sub>, and references 208a, 208b, 208c, and 208d indicate control gate electrodes. Fig. 2(b) shows a further simplified version of this for the purposes of analyzing the operation of the nu MOS. If the capacitive coupling coefficients between each control gate electrode and the floating gate are represented by C1, C2, C3, and C4, as in the figure, and the capacitive coupling coefficient between the floating gate and the silicon substrate is represented by C0, then the potential PHI F of the floating gate is given by the following formulas.

$$(1) \text{ PHI F} = (1/CTOT) (C1V1 + C2V2 + C3V3 + C4V4)$$

$$(2) \text{ Here, } CTOT = C0 + C1 + C2 + C3 + C4$$

V1, V2, V3, and V4 indicate voltages which are applied to, respectively, input gates 208a, 208b, 208c, and 208d, and the potential of the silicon substrate is 0V, so that it is grounded.

Now, the potential of source 202 is set to 0V. That is to say, it is set to a value in which the potentials of all the electrodes are measured using the source as a standard. In this way, if the floating gate 206 is seen as a standard gate electrode, the nu MOS shown in Fig. 2 becomes equivalent to a standard N-channel MOS transistor, and when the gate potential PHI F thereof exceeds a threshold value (VTH\*), the source and the drain become electrically connected. That is to say, from formula (1), the nu MOS becomes conductive (enters an ON state) when the following conditions are met.

$$(3) (CTOT) (C1V1 + C2V2 + C3V3 + C4V4) > VTH^*$$

The foregoing explanation referred to an N-channel MOS transistor; however, there are devices having the structure shown in Fig. 2(a) in which the source 202, the drain 203, and the substrate 201 are all of the opposite conductivity type. That is to say, such a nu MOS has an N-type substrate, and the source and drain are formed from P diffusion layers, and this is termed a "P-channel MOS transistor".

#### Neuron Circuit, Soft-Hardware Logical Circuit

Next, the most fundamental circuit used in the nu MOS, the neuron circuit, and the operation thereof will be explained using Fig. 3. The neuron circuit comprises a nu MOS inverter 212, comprising a N-channel nu MOS 210 and a P-channel nu MOS 211, and a standard inverter 213. This circuit is such that the nu MOS inverter inverts when the potential PHI F of the common floating gate 214 exceeds the inversion voltage (1/2) VDD of the nu MOS inverter, and VOUT becomes "1". In the figure, the capacitive coupling coefficients of the V1 SIMILAR V4 gates are all set to (1/8) CTOT, and the capacitive coupling coefficient of the VP gate is set to (1/2) CTOT, and for the purposes of simplicity, it is assumed that C0 = 0. The VP gate is termed the "main electrode" of the nu MOS inverter.

It is possible to analyze the operation of this circuit in a simple manner by means of the floating gate potential diagram (abbreviated to "FPD") shown in Fig. 4. the FPD depicts PHI F as a function of VP, and if V1 SIMILAR V4 = 0, then when VP changes from 0 to VDD, PHI F changes from 0 to (1/2) VDD. This is because the coupling capacity of VP is (1/2) CTOT. That is to say, the potential of the neuron circuit is constantly 0.

In the example shown in Fig. 4,  $V_1 = V_2 = 0$ ,  $V_4 = V_{DD}$ , and  $V_3$  has a value of  $V_{DD}$  when  $V_P$  is within a range of 0 SIMILAR  $(3/4) V_{DD}$ , and a value of 0 when  $V_P > (3/4) V_{DD}$ . In this way,  $\Phi F$  is such that a value of  $V_{OUT}$  of 1 is outputted when  $V_P > (1/2) V_{DD}$ . In order to realize such a circuit, as shown in Fig. 5,  $V_P$  may be passed through a pre-inverter 214 having a threshold value of  $(3/4) V_{DD}$  before being inputted into  $V_3$ . Such circuits are the basis of the soft-hardware logic circuits (abbreviated to "SHL").

Next, an example of an SHL circuit will be explained using Figs. 6 and 7. In Fig. 6, a circuit diagram is shown. Reference 301 indicates a D/A converter which is provided at the input stage; this generates a 4-level multivalent variable  $V_P$  with respect to combinations of two inputs  $X_1$  and  $X_2$ .  $V_P$  is inputted into the main gate of the 5 nu MOS inverters 302 SIMILAR 306. The relationships between  $X_1$  and  $X_2$  and  $V_P$  are shown on the horizontal axis of the FPDs shown in Fig. 7(a).  $V_a$ ,  $V_b$ ,  $V_c$ , and  $V_d$  correspond to, for example, the control signal input terminals 104a SIMILAR 104d of the operational block A of Fig. 1. In the figure, the fractions such as  $1/2$ ,  $1/4$ ,  $1/8$ , and the like, indicate the capacitive coupling coefficients between the respective input gates and the floating gate, and these indicate, respectively,  $(1/2) CTOT$ ,  $(1/4) CTOT$ ,  $(1/8) CTOT$ , and the like.

In the present circuit, signals having the two values of 0 or  $V_{DD}$  are inputted into  $V_a$ ,  $V_b$ ,  $V_c$ , and  $V_d$ . The case in which  $V_a = V_b = V_c = V_d = 1 (= V_{DD})$  is shown in the FPD of nu MOS inverter 302 which is shown in Fig. 7(a). The FPDs of  $V_a$ ,  $V_b$ ,  $V_c$ , and  $V_d$  relating to other combinations, and examples of outputs are shown in Fig. 7(a), (b), (c), and (d). It can be seen that the inversion signals of the signals inputted into  $V_a$ ,  $V_b$ ,  $V_c$ , and  $V_d$  are outputted in response to  $(X_2, X_1) = (0, 0)$ ,  $(0, 1)$ ,  $(1, 0)$ , and  $(1, 1)$ . It is possible to designate the output pattern and to determine the form of the function directly by means of  $V_a$ , SIMILAR  $V_d$ , so that the determination of the function can be easily conducted, and this is a major characteristic feature.

The circuit shown in Fig. 6 is only an example of an SHL, and it is of course the case that it is possible to use other SHLs which are described in the patent specification (Japanese Patent Application No. Hei 3-83135).

## (Embodiment 2)

Next, a second embodiment of the present invention is shown in Fig. 8. This is a computing circuit which employs one nu MOS inverter as an operating block and comprises 8 such blocks; it is a binary SD number adder. Conventionally, when conducting addition operations, addition was conducted starting with the least significant bit, carrying the result after each calculation, and proceeding to the next bit, so that when the bit length was long, there was an operational period delay in proportion to this. This constituted a great hindrance to high-speed operational processing.

The present embodiment realizes an adder in which the carry over only affects the immediately following place, so that there is no so-called "carry over propagation"; this is realized in a simple manner for the first time by using SHL circuits, and altering the functions of a portion of the circuit blocks using a portion of the operational results. Prior to the explanation of the present embodiment, the SD numerical system will be explained.

The Signed-Digit (SD) numerical system [1] is a numerical system which expresses signals having a plurality of values. What is meant by an "SD numerical system" is a method of expression having a large expressive capacity; for this reason, it has superior characteristic features. For example, in an SD number adder, the carry propagation is limited to one stage irrespective of word length, so that operations proceed essentially in parallel. If this characteristic feature is taken advantage of, high speed operation becomes possible.

What is meant by a "binary SD number" is the number  $X$  which is defined as shown below.

$$X = a_{n-1} 2 + a_{n-2} 2 + \dots + a_1 2 + a_0$$

$a_i \in \{-1, 0, 1\}$

That is to say, in this numerical system, one place (one bit) can have 3 values; however, this is a binary number, not a base 3 number. That is to say, the numerical system has a larger expressive capacity. For example,  $(1, -1, 0)$  and  $(0, 1, 0)$  can be expressed by the same binary SD number. Consideration will now be given to the addition of SD numbers. The i-place of 2 binary SD numbers will be represented

by  $x_i$  and  $y_i$ , and the linear sum thereof is represented by  $z_i$ .

$x_i$  ELEMENT  $\{-1, 0, 1\}$

$y_i$  ELEMENT  $\{-1, 0, 1\}$

$z_i = x_i + y_i$  ELEMENT  $\{-2, -1, 0, 1, 2\}$

With respect to this  $z_i$ , a carry  $c_i$  and an intermediate sum  $w_i$  in accordance with the following formula:

$z_i = 2c_i + w_i$

$c_i, w_i$  ELEMENT  $\{-1, 0, 1\}$

are determined; however, at this time, the carry and intermediate sum may be determined under the conditions shown in Table 1 in consideration of the linear sum  $z_{i-1}$  of the less significant bit.

Id=Table 1 Columns=4 Table of the true values of the carry  $c$  and the intermediate sum  $w$  of an SD adder.

Head Col 1:  $z_i$

Head Col 2:  $z_{i-1}$

Head Col 3:  $c_i$

Head Col 4:  $w_i$

2\*10

1 (SEP)/= 01-1

< 001

0\*00

-1< 0-11

(SEP)/= 00-1

-2\*-10

If the intermediate sum  $w_i$  and the carry  $c_{i-1}$  obtained from the less significant bit which are obtained here are added in a linear manner, the final sum  $s_i$  is obtained. During the determination of the conditions described above, a carry is generated in consideration of the linear sum of the less significant bit, so that there is no carry over generated in the calculation which obtains the final sum. Accordingly, carry propagation is limited to the adjacent bit. The foregoing is the SD numerical additional algorithm.

In order to realize this algorithm using nu MOS, first, binary SD numbers having 3 values were coded into 2-bit binary numbers. This is because when a nu MOS inverter is employed, the output of the inverter has two values. Tables 2 and 3 show coding tables.

Id=Table 2 Columns=3 Coding of binary SD numbers and 2-bit binary numbers

Head Col 1: Binary SD

Head Col 2 to 3: Binary Number

111

001

-100

Id=Table 3 Columns=2 Coding of the linear sum  $w$

Head Col 1:  $z$

Head Col 2:  $x + y$

2Four 1's

1Three 1's

0Two 1's

-1One 1

-2One 1

When transforming SD numbers having three values into 2-bit binary numbers, coding was conducted focusing on the number of 1's. With respect to  $z$ , which is the linear sum of  $x$  and  $y$ , this was coded by one number contained between  $x$  and  $y$ . The true value table of the SD addition described above is rewritten in accordance with this coding. Furthermore, the true value table divided into two based on whether  $z_{i-1}$ , which is the linear sum of the less significant place, is greater than or equal to 0, or less than 0.

The rewritten true value table is shown in Table 4.

Here, what is meant by the "control signal" is a variable which takes a value of "1" when the linear sum  $z_{i-1}$  of the less significant bit is "0" or more, and takes a value of "0" when this sum is less than "0". With respect to  $c_i$  and  $w_i$  in the true value table, the left-hand column divided by a dotted line represents the more significant bit, while the right hand column represents the less significant bit.

The circuit diagram of Fig. 9 shows a realization of the true value table shown in Table 4 using nu MOS logic circuits. This figure depicts the circuit blocks 401 SIMILAR 404 of Fig. 8; the circuit outputs the inverted signals of carry  $C_i$  and the sum  $W_i$ , respectively, of  $X_i$  and  $Y_i$ .

A symmetrical function nu MOS logic circuit having a total of 4-bit inputs, the two bits of input  $x$  and the two bits of input  $y$ , is employed. The number of 1's, which is the result of the coding of  $z$ , is employed in an unchanged manner as the main variable  $V_p$  of the nu MOS inverter. Figs. 10, 11, 12, and 13 show FPDs of nu MOS inverters 401 SIMILAR 404, in which the number of 1's within  $Z$  is depicted as the main variable  $V_p$ .

For example, in the nu MOS inverter which calculates the more significant bit of carry  $c$  (Fig. 10), when the control signal CTRL is "0", "00001" is set as the target function (the output characteristics), and when the control function is "1", the target function is set to "00011". That is to say, the input terminal 405 of the control signal CTRL functions as a control signal input terminal which controls the operating function of operational blocks 401 and 402. The terminal 406 into which  $x_i$  and  $y_i$  are inputted is a data signal input terminal. In Figs. 10 SIMILAR 13, the form of the function when CTRL = 1 is shown by the dotted line and the shaded area (407c SIMILAR f), while the form of the function when a CTRL = 0 is shown by the solid line (408c SIMILAR f).

In this way, the SD number adder (SDFA) circuit shown in Fig. 9 is realized. In order to simplify the circuit, carry  $c$  and intermediate sum  $w$  are outputted as inverted values. The nu MOS inverter which calculates the more significant bit of the carry described above is the left-most inverter 401. Here, consideration will be given to the nu MOS inverter 403 which calculates the more significant bit of the intermediate sum  $w$ . When the control signal is "0", the target function of this neuron circuit is "01010". This is an XOR function. When the control signal is "1", the target function is "00000". In this way, in order to calculate the more significant bit of the intermediate sum  $w$ , this nu MOS inverter operating unit has a function which is changed when an XOR function is calculated by means of the control signal CTRL, or when, irrespective of input, a value of "0" is outputted. Here, the output of nu MOS inverters 401 and 402 which calculate the carry is inputted into the control signal input terminal 409 which determines the function of operating units 403 and 404, and the function thereof can be changed where necessary. By means of this, the calculation of the intermediate sum is realized.

Fig. 14 shows all the circuitry corresponding to one decimal place which conducts the addition of the binary SD numbers. The control signal CTRL is produced by means of a control circuit comprising one nu MOS inverter (410) and one standard inverter (411). Furthermore,  $s$ , which represents the final addition result, is obtained by conducting the addition of the intermediate sum  $w$  and the carry from the less significant place by means of a linear adder 414, comprising 2 nu MOS inverters 412 and 413.

In the above manner, a binary SD number adder can be constructed in an extremely simple manner by means of the present invention. The number of transistors required is only 16 per decimal place, and this was heretofore not realizable by means of such simple circuitry.

The binary SD number adder described above is a circuit which outputs signals in which binary SD numbers are coded in 2-bit binary numbers. If the binary SD numbers are expressed as positive voltage values, these can be directly coupled to the floating gate of the nu MOS inverter as signals having three values. Furthermore, the output may be outputted after converting the 2-bit binary output to a three-value SD number at the nu MOS source follower circuit. That is to say, the SD adder described in the present embodiment is a circuit which is capable of easy interface with binary signals and signals having a plurality of values, so that it has an extremely broad range of applications.

(Embodiment 3)

A third embodiment of the present invention is shown in Fig. 15. Here, a representative example employing an operating unit A having a number  $n$  of input terminals for data signals is shown. The output of unit A is applied to flip-flop 502, and the output thereof is again applied to the portion 503 of the control input terminal which determines the function of the unit A itself. This flip-flop may also be a

shift register which is controlled by means of a clock. When the output of A has a predetermined delay applied thereto and is then inputted into the control input terminal in this manner, the function thereof changes based on the past operation results. That is to say, the output of the unit itself is subjected to feedback and determines the function thereof. By means of adding this type of memory function, it is possible to provide an even wider range of operating functions.

The output of the memory element or a delay element 502 may be inputted into the control input terminal 505 of a unit B (504) different from the unit A, in the manner shown in Fig. 16.

(Embodiment 4)

Fig. 6 shows a fourth embodiment of the present invention; the output of A is inputted into a binary counter 506. This is an example in which the number of times A has a value of "1" is counted, and the three bits into which this number is encoded in a binary fashion are applied to the determination of the function. It is of course the case that in this case as well, this may be used in order to determine the function of other blocks.

In accordance with the present invention described above, the circuit itself may change structure or produce new functions based on its own operational results, so that it is possible to realize flexible information processing analogous to that of living things, such as learning, adaptation, and self-multiplication, which are necessary in a society dealing with a high level of information. Additionally, it is possible to realize computers having completely different algorithms and architecture from those which have previously existed.

In the foregoing, only that case was shown in which the floating gate of the nMOS inverter was in a constantly floating state; however, as shown in Fig. 18, a switch transistor 701 may be added to the floating gate, and a given voltage  $V_m$  may be connected. Alternatively, the value of this potential may be employed as other data. Furthermore, the signal  $V_s$  which controls the switch may of course be synchronized with a system clock, and the charge within the floating gate may be returned to the original state each time, or the current flowing to the inverter may be cut, or the like.

#### Industrial Applicability

By means of the present invention, it is possible to realize a novel computing and processing device which is capable of flexible information processing analogous to that of living things, such as learning, adaptation, and self-multiplication, and high level information processing is possible.

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### Claims

1. A computing device, comprising a plurality of first input terminals and a plurality of second input terminals, and a plurality of operational units which execute given operations, stipulated by means of control signals inputted into said second input terminals, with respect to data signals inputted into said first input terminals, and which each have at least one output terminal for outputting results thereof; characterized in that the output signal outputted from one of said output terminals or the result of a given operational processing of this output signal, is inputted into at least one of said second input terminals.
2. A computing device in accordance with Claim 1, characterized in that said operational units contain inverters comprising at least one stage of neuron MOS transistors.

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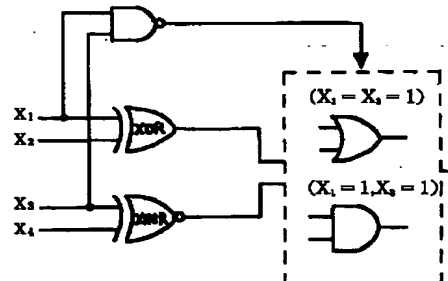
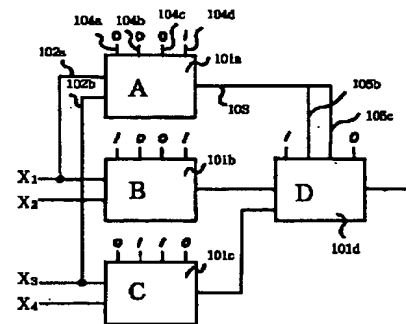
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(54)【発明の名称】 演算装置

(57)【要約】

【目的】 本発明は、今後の高度な情報処理実現に必須な学習、適応、自己増殖といった生命体と類似の柔軟な情報処理を可能にする新しい演算装置を提供することを目的とする。

【構成】 複数の第1の入力端子と複数の第2の入力端子を有し、前記第1の入力端子に入力されるデータ信号に対し前記第2の入力端子に入力される制御信号によって規定される所定の演算処理を行い、その結果を出力する出力端子を少なくとも1つ有する演算ユニットを複数個、有する演算装置において、前記出力端子の1つより出力された出力信号もしくは該出力信号に所定の演算処理を行った結果が、前記第2の入力端子の少なくとも1つに入力されていることを特徴とする。



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## 【特許請求の範囲】

【請求項1】 複数の第1の入力端子と複数の第2の入力端子を有し、前記第1の入力端子に入力されるデータ信号に対し前記第2の入力端子に入力される制御信号によって規定される所定の演算処理を行い、その結果を出力する出力端子を少なくとも1つ有する演算ユニットを複数個、有する演算装置において、前記出力端子の1つより出力された出力信号もしくは該出力信号に所定の演算処理を行った結果が、前記第2の入力端子の少なくとも1つに入力されていることを特徴とする演算装置。

【請求項2】 前記演算ユニットは、少なくとも1段のニューロンMOSトランジスタで構成されたインバータを含んでいることを特徴とする請求項1に記載の演算装置。

## 【発明の詳細な説明】

【0001】

【産業上の利用分野】 本発明は情報処理技術に係わり、特に柔軟な情報処理を可能とする演算装置に関する。

【0002】

【背景技術】 従来、情報処理技術を行うコンピュータの心臓部のCPUは半導体LSIで構成されているが、これらはハードウェアと呼ばれている。この理由は一度作ってしまえばその構造は不変であり、変えることができない堅固なものだからである。コンピュータが様々な機能をはたしているのは、プログラムによって機能の固定された回路に仕事を順序よく実行させているに過ぎない。しかし、今後の高度な情報処理が実現するためには人間が行っているような学習や適応あるいは自己増殖といった生命体自身が行っているような情報処理にも対応できるものでなければならないが、現在のところこのようなコンピュータ存在しない。

【0003】 一方、ソフトウェア技術によって柔軟な情報処理を実現しようという試みも盛んに行われているが、なかなかうまくできないのが現状である。その理由は、もともと融通の効かないハードウェアをベースにしているためであり、擬似的に実現してもソフトウェアの負担が過大となり、スーパーコンピュータをもってしても多大な時間を要し、とても瞬時に応答するシステムは構築できない。

【0004】 これを解決する1つの有力な方法として、脳の情報処理そのものを真似たいわゆるニューラルネットワークが研究開発されているが、これも未だ実用化にはほど遠い状態である。その理由は、脳の情報処理の本質がほとんど分かっていない状況で、非常に原始的な構造を真似ているだけであり、具体的な論理の構築方法等は皆無の状態である。

【0005】 これに対し、ニューロンMOSトランジスタ（発明者：柴田 直、大見忠弘、特開平3-6679号公報）という高機能トランジスタが発明され、これを応用したソフトハードウェア回路（発明者：柴田 直、

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大見忠弘：特願平3-83135号）が発明された。特にこのソフトハードウェア回路は外部信号によってその演算機能を自由自在に変更することができる非常に柔軟なハードウェアを有する回路である。この様な柔軟なハードウェアをベースにすれば、冒頭に述べた柔軟な情報処理を実現できる可能性があるが、これまでその方法は明らかにされていなかった。

【0006】

【発明が解決しようとする課題】 そこで本発明は、今後の高度な情報処理実現に必須な学習、適応、自己増殖といった生命体と類似の柔軟な情報処理を可能にする新しい演算装置を提供することを目的とする。

【0007】

【課題を解決するための手段】 本発明の演算装置は、複数の第1の入力端子と複数の第2の入力端子を有し、前記第1の入力端子に入力されるデータ信号に対し前記第2の入力端子に入力される制御信号によって規定される所定の演算処理を行い、その結果を出力する出力端子を少なくとも1つ有する演算ユニットを複数個有する演算装置において、前記出力端子の1つより出力された出力信号もしくは該出力信号に所定の演算処理を行った結果が、前記第2の入力端子の少なくとも1つに入力されていることを特徴とする

【0008】

【実施例】 以下本発明の実施例を図面を用いて説明する。

【0009】（実施例1）図1（a）は本発明の第1の実施例を示すブロックダイアグラムである。この回路は、 $X_1 \sim X_4$ の4つのデジタル入力信号に対し次の演算処理を行う。もし、 $X_1 = X_3 = 1$ ならば、 $X_2 = 0$ もしくは $X_4 = 1$ の時に1を出力し、それ以外の場合、即ち $X_1$ か $X_3$ のどちらかが1に等しくない場合は、 $X_1 \neq X_2$ で且つ $X_3 = X_4$ の時のみ1を出力する演算装置である。

【0010】 本回路は、A、B、C、D（101a～101d）4つの論理演算ユニットを互いに配線まで接続することによりできている。各演算ユニットは、2つの入力端子（102a、102b等）と1つの出力端子103及び4つの制御信号入力端子（104a、104b、104c、104d等）を有しており、その演算機能は制御入力端子に入力される0もしくは1の信号で規定される。0は0V、1は電源電圧 $V_{DD}$ （5V）をそれぞれ入力端子を加えることを意味している。このような回路は、例えばニューロンMOSトランジスタ（特開平3-6679号公報）を用いたソフトハードウェア論理回路（特願平3-83135号）を用いれば良い。ニューロンMOSトランジスタとソフトハードウェア論理回路については別途説明する。

【0011】 A、B、Cの各ブロックは図に示した制御入力端子（104a～104d）への入力信号によりそれぞれNAND回路、XOR回路、XNOR回路となっ

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て位いる。ブロックDは、その2つの制御入力端子105b, 105cは一定の信号ではなく、ブロックA(NAND回路)の出力がそのまま入力されているため、その出力103が0ならばOR回路、1ならばAND回路となる。この関係を分かりやすく示したのが図1(b)である。

【0012】ブロックDに相当する部分が、 $X_1$ と $X_3$ のNAND演算の結果によって異なった機能をもつように構成されている。

【0013】以上に示したように、本実施例では、回路がその演算結果によってその回路自身の一部の機能を変化させ全体の機能を変化させることにより、柔軟な演算機能を実現している。

【0014】以上極めて簡単な場合を例示したため、新しい柔軟な機能の重要性は必ずしも明かではないが、これに関してはニューロンMOSトランジスタ並びにソフトハードウェア論理回路についてそれぞれ図2~7を用いて説明した後、第2の実施例にて詳述する。

$$\phi_F = (1/C_{TOT}) (C_1 V_1 + C_2 V_2 + C_3 V_3 + C_4 V_4) \quad (1)$$

$$\text{但し、} C_{TOT} = C_0 + C_1 + C_2 + C_3 + C_4 \quad (2)$$

$V_1, V_2, V_3, V_4$ はそれぞれ入力ゲート208a, 208b, 208c, 208dに印加されている電圧であり、シリコン基板の電位は0V、即ちアースされているとした。

【0017】今、ソース202の電位を0Vとする。即ち、全ての電極の電位をソースを基準として測定した値※

$$(C_{TOT}) (C_1 V_1 + C_2 V_2 + C_3 V_3 + C_4 V_4) > V_{TH}^* \quad (3)$$

の条件が満たされたとき、 $\nu$ MOSは導通(ONする)のである。

【0018】以上はNチャネルMOSトランジスタについての説明であるが、図2(a)においてソース202、ドレイン203及び基板201を全て反対導電型にしたデバイスも存在する。即ち、基板はN型であり、ソース・ドレインがP+拡散層で形成された $\nu$ MOSであり、これをPチャネルMOSトランジスタと呼ぶ。

【0019】ニューロン回路、ソフトハードウェア論理回路

次に $\nu$ MOSを用いた最も基本的な回路、ニューロン回路とその動作について図3を用いて説明する。ニューロン回路は、Nチャネル $\nu$ MOS210とPチャネル $\nu$ MOS211より構成された $\nu$ MOSインバータ212及び通常インバータ213よりできている。この回路は、共通のフローティングゲート214の電位 $\phi_F$ が $\nu$ MOSインバータの反転電圧 $(1/2)V_{DD}$ を越えたときに $\nu$ MOSインバータが反転し、 $V_{OUT}$ が1となる回路である。図において、 $V_1 \sim V_4$ ゲートの容量結合係数は全て $(1/8)C_{TOT}$ 、 $V_p$ ゲートのそれは $(1/2)C_{TOT}$ とし、簡単のため $C_0 = 0$ と仮定した。 $V_p$ ゲートは $\nu$ MOSインバータの主要電極と呼ぶ。

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\*【0015】まず最初にニューロンMOSトランジスタ(以下 $\nu$ MOSと略す)の構造と動作原理について説明する。図2は4入力のNチャネル $\nu$ MOSトランジスタの断面構造の一例を示したものであり、201は例えばP型のシリコン基板、202、203はN+拡散層で形成されたソース及びドレイン、204はソース・ドレイン間のチャネル領域205上に設けられたゲート絶縁膜(例えば $SiO_2$ 膜)、206は電気的に絶縁され電位的にフローティングの状態にあるフローティングゲート電極、207は例えば $SiO_2$ 等の絶縁膜、208a, 208b, 208c, 208dは制御ゲート電極である。図2(b)は、 $\nu$ MOS動作を解析するために更に簡略化した図面である。各制御ゲート電極とフローティングゲート間の容量結合係数を図のように $C_1, C_2, C_3, C_4$ 、フローティングゲートとシリコン基板間の容量結合係数を $C_0$ とすると、フローティングゲートの電位 $\phi_F$ は次式で与えられる。

\*【0016】

※とする。そうすれば、図2に示した $\nu$ MOSはフローティングゲート206を通常のゲート電極とみなせば通常のNチャネルMOSトランジスタと同じであり、そのゲート電位 $\phi_F$ が閾値( $V_{TH}^*$ )より大となると、ソース・ドレイン間が電気的に接続される。即ち、(1)式より

【0020】この回路の動作は、図4に示したフローティング・ゲート・ポテンシャル図(Floating-Gate Potential Diagram = FPDと略称)によって簡単に解析することができる。FPDは $\phi_F$ を $V_p$ の関数として表したもので、 $V_1 \sim V_4 = 0$ ならば、 $V_p$ が0から $V_{DD}$ まで変化したとき $\phi_F$ は0から $(1/2)V_{DD}$ まで変化する。それは $V_p$ の結合容量は $(1/2)C_{TOT}$ だからである。つまりニューロン回路の出力は常に0である。

【0021】図4の例では、 $V_1 = V_2 = 0, V_4 = V_{DD}$ で、 $V_3$ は $V_p$ が0 $\sim (3/4)V_{DD}$ まで $V_{DD}$ で、 $V_p > (3/4)V_{DD}$ で0となる場合が図示してある。こうすれば、 $\phi_F$ は $V_p > (1/2)V_{DD}$ で $V_{OUT}$ は1を出力するようになっている。このような回路を実現しようと思えば、図5に示したように $V_p$ を閾値が $(3/4)V_{DD}$ のブレインバータ214を通してから $V_3$ に入力してやれば良い。同様な回路がソフトハードウェア論理回路(Soft Hardware Logic回路=SHLと略称)の基本となっている。

【0022】次にSHL回路の一例について、図6, 7を用いて説明する。図6にその回路図を示した。301は入力段に設けられたD/A変換器で、2つの入力

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$X_1$ ,  $X_2$ の組み合わせに対し4レベルの多値変数 $V_0$ を発生する。 $V_0$ は、5つの $\nu$ MOSインバータ302~306の主要ゲートに入力されている。 $X_1$ ,  $X_2$ と $V_0$ の関係は、図7(a)のFPDの横軸に示されている。 $V_1$ ,  $V_2$ ,  $V_3$ ,  $V_4$ は、例えば図1の演算ブロックAの制御信号入力端子104a~104dに対応している。図に $1/2$ ,  $1/4$ ,  $1/8$ 等の分数が示してあるのは、各入力ゲートとフローティングゲート間の容量結合係数であり、それぞれ $(1/2)C_{107}$ ,  $(1/4)C_{107}$ ,  $(1/8)C_{107}$ 等を意味している。

【0023】本回路では、 $V_1$ ,  $V_2$ ,  $V_3$ ,  $V_4$ は、0または $V_{DD}$ の2値信号が入力される。 $\nu$ MOSインバータ302のFPDを $V_1=V_2=V_3=V_4=1$ (= $V_{DD}$ )の場合について示したのが図7(a)である。出力は全ての入力の組み合わせに対して0となる。 $V_1$ ,  $V_2$ ,  $V_3$ ,  $V_4$ のその他の組み合わせに対するFPD及び出力の一例を図7(a), (b), (c), (d)に示した。 $V_1$ ,  $V_2$ ,  $V_3$ ,  $V_4$ に入力した信号の反転信号が $(X_2, X_1) = (0, 0)$ ,  $(0, 1)$ ,  $(1, 0)$ ,  $(1, 1)$ に対応して出力されていることが分かる。出力パターンを直接 $V_1 \sim V_4$ によって指定して、関数形を決めることができるため、関数の決定が容易に行えることが大きな特徴である。

【0024】図6の回路はあくまでSHLの一例であり、特許明細書(特願平3-83135号)に記載されているその他のSHLを用いても良いことは言うまでもない。

【0025】(実施例2)次に本発明の第2の実施例を図8に示す。これは $\nu$ MOSインバータ1つを演算ブロックとし、8ケのブロックから構成された演算回路であり、2進SD数加算器となっている。従来、加算演算を行う際には、一番下位のビットから加算を行い、その都度ケタ上げ(キャリ)を計算してから上のビットの計算へと進んで行くため、ビット長が長くなると、それに比例して演算時間の遅れが大きくなっていた。これが高速演算処理を行う際の大きな障害となっていた。

【0026】本実施例は、ケタ上げがすぐとなりのケタ

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にしか影響を与えない、いわゆるキャリ伝搬の無い加算器を実現したものであり、SHL回路を用い、演算の結果を一部用いて、一部の回路ブロックの機能を変更することにより初めて簡単に実現できたものである。本実施例の前にまずSD数系について説明する。

【0027】多値の信号を表現する数系の一つが、Signed-Digit (SD) 数系[1]である。SD数系とは、冗長性を持った表現法であるが、それ故に、優れた特徴を持っている。たとえば、SD数の加減算では、ワード長に関係なくキャリの伝搬が1段のみに限定され、ほぼ並列に演算が進行する。この特徴を生かせば、高速演算が可能となる。

【0028】2進SD数とは、以下のように定義される数 $X$ である。

$$X = a_{n-1} 2^{n-1} + a_{n-2} 2^{n-2} + \dots + a_1 2 + a_0$$

$$a_i \in \{-1, 0, 1\}$$

つまり、1桁(1ビット)が3値の値をとる数系であるが、3進数ではなく2進数である。つまり冗長な数系である。例えば2進SD数で、 $(1, -1, 0)$ は、 $(0, 1, 0)$ と同じ数を示している。このような、SD数の加算を考える。2つの2進SD数の1桁を $x_i$ ,  $y_i$ , およびその線形加算和を $z_i$ とする。

$$【0029】 x_i \in \{-1, 0, 1\}$$

$$y_i \in \{-1, 0, 1\}$$

$$z_i = x_i + y_i \in \{-2, -1, 0, 1, 2\}$$

この $z_i$ に対して、

$$z_i = 2c_i + w_i$$

$$c_i, w_i \in \{-1, 0, 1\}$$

を満足するキャリ $c_i$ と中間和 $w_i$ を求めるわけであるが、この時、下位ビットの線形加算和 $z_{i-1}$ を考慮して表1に示される条件でキャリおよび中間和を求めればよい。

【0030】

【表1】 SD加算器のキャリ $c$ および中間和 $w$ の真理値表

$z_i$	$z_{i-1}$	$c_i$	$w_i$
2	*	1	0
1	$\geq 0$ $< 0$	1 0	-1 1
0	*	0	0
-1	$< 0$ $\geq 0$	-1 0	1 -1
-2	*	-1	0

ここで求まった中間和 $w_i$ と下位ビットからのキャリ $c_{i-1}$ を線形加算すれば、最終的な和 $s_i$ が求められる。上記条件判断の時に下位ビットの線形加算和を考慮してキャリを発生させているので、最終的な和を求める演算で桁上げキャリが発生する事はない。したがって、キャリの伝搬は隣合ったビット間のみに限定される。以上がSD数加算のアルゴリズムである。

【0031】このアルゴリズムを $\nu$ MOSで実現するために、まず、3値の2進SD数を2ビットの2進数にコーディングを行った。これは、 $\nu$ MOSインバータを用いる場合に、インバータの出力は2値となるためである。コーディングを表2および表3に示す。

【0032】

【表2】 2進SD数と2ビット2進数のコーディング

2進SD	2進数	
1	1	1
0	0	1
-1	0	0

【0033】

【表3】 線形加算和 $w$ のコーディング

$z$	$x+y$
2	1が4個
1	1が3個
0	1が2個
-1	1が1個
-2	1が0個

3値のSD数を2ビットの2進数にするときには、1の個数に注目してコーディングを行った。 $x$ と $y$ の線形加算和である $z$ に関しては、 $x$ と $y$ のなかに含まれる1の数でコーディングした。このコーディングにしたがって前述のSD加算の真理値表を書き換える。また、下位桁の線形加算和である $z_{i-1}$ が0以上か0未満かで真理値表を2つに分離する。書き換えられた真理値表を表4に示す。

【0034】

【表4】  $\nu$ MOS論理回路用に書き換えられた真理値表

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(a) 制御信号が1の時 ( $z_{i-1} \geq 0$ ) (b) 制御信号が0の時 ( $z_{i-1} < 0$ )

z i	c i		w i	
1が4個	1	1	0	1
1が3個	1	1	0	0
1が2個	0	1	0	1
1が1個	0	1	0	0
1が0個	0	0	0	1

z i	c i		w i	
1が4個	1	1	0	1
1が3個	0	1	1	1
1が2個	0	1	0	1
1が1個	0	0	1	1
1が0個	0	0	0	1

ここで、制御信号とは、下位ビットの線形加算和  $z_{i-1}$  が0以上であれば1、0未満であれば0をとる変数である。真理値表中で  $c_i$ 、 $w_i$  に関しては、点線で区切られた左の欄が上位ビット、右の欄が下位ビットを示す。

【0035】表4で示された真理値表を、 $\nu$ MOS論理回路を用いて実現したものが図9に回路図で示されている。これは図8の回路ブロック401~404を取り出して描いたものであり、 $X_i$ 、 $Y_i$  に対し、キャリ  $C_i$  と  $W_i$  それぞれの反転信号を出力する回路である。

【0036】入力  $x$  の2ビットおよび  $y$  の2ビットの計4ビット入力の対称関数  $\nu$ MOS論理回路を用いる。 $z$  のコーディングされた結果である1の個数が、そのまま  $\nu$ MOSインバータの主要変数  $V_i$  となる。 $\nu$ MOSインバータ401~404のFPDを、 $Z$  中の1の個数を主要変数  $V_i$  として描いたものをそれぞれ図10、11、12、13に示す。

【0037】例えば、キャリ  $c$  の上位ビットを演算する  $\nu$ MOSインバータ(図10)においては、ターゲット関数(出力の特性)として、制御信号  $CTRL$  が0のとき00001、制御関数が1のとき、00011を設定すればよいことになる。つまり制御信号  $CTRL$  の入力端子405が、演算ブロック401、402の演算機能を決定する制御信号入力端子の働きをしている。 $X_i$ 、 $Y_i$  の入力される端子406はデータ信号入力端子である。図10~13で、点線とハッチ(407c~f)で示したのが、 $CTRL=1$  の場合の関数形であり、実線(408c~f)で示したのが、 $CTRL=0$  の場合の関数形である。

【0038】このようにして図9のSD数加算器(SDFA)回路が実現されている。回路の簡単化のため、キャリ  $c$  および中間和  $w$  は反転(否定)値で出力してある。前述のキャリの上位ビットを演算する  $\nu$ MOSインバータは、一番左のインバータ401である。ここで、中間和  $w$  の上位ビットを演算する  $\nu$ MOSインバータ403について考える。このニューロン回路は、制御信号が0のとき、ターゲット関数が01010となる。これはXOR関数である。ところが制御信号が1のときはターゲット関数は00000となる。このように、中間和

$w$  の上位ビットを演算するために、この  $\nu$ MOSインバータ演算ユニットは、制御信号  $CTRL$  によってXOR関数を演算したり、入力に関わらず0を出力したりと、その関数を変えているのである。ここでは、キャリを演算する  $\nu$ MOSインバータ401、402の出力が演算ユニット403、404の機能を決定する制御信号入力端子409に入力され、その機能を必要に応じて変更しているのである。これにより、中間和の演算を実現している。

【0039】図14は2進SD数の加算を行う回路の1桁分を全て表示している。制御信号  $CTRL$  は、 $\nu$ MOSインバータ1個(410)と通常インバータ(411)1個で構成された制御回路によって作り出されている。また、最終的な加算結果である  $s$  は、中間和  $w$  と下位桁からのキャリの加算を  $\nu$ MOSインバータ2個(412、413)で構成された線形加算器(414)で行う事により得られる。

【0040】以上のように、2進SD数の加算器が本発明により、非常に簡単に構成できた。なお、必要とされるトランジスタ数は、1桁当たり、たったの16個であり、これまでこのように簡単な回路で実現することは、全く不可能であった。

【0041】以上述べた2進SD数加算器は、2進SD数を2ビットの2進数にコーディングした信号を入出力する回路である。ところが、正の電圧値で表された2進SD数であれば、3値信号のまま直接  $\nu$ MOSインバータのフローティングゲートに結合する事が可能である。また、出力は、2ビットのバイナリ出力を  $\nu$ MOSソースフォロア回路で3値のSD数に変換してから出力する事も可能である。つまり、本実施例で述べたSD加算器は、バイナリ信号、および多値の信号ともに容易にインターフェイスが可能な回路であり極めて汎用性に富んでいる。

【0042】(実施例3) 本発明の第3の実施例を図15に示す。ここでは一般的に  $n$  個のデータ信号用入力端子501を有する演算ユニットAを用いて代表例が示してある。ユニットAの出力は、フリップ・フロップ502にたくわえられ、その出力が再びユニットA自身の機

能を規定する制御入力端子の一部503に加えられている。このフリップ・フロップはクロックにより制御されたシフトレジスタでも良い。こうしてAの出力に所定の遅れを入れて、制御入力端子に入れてやると、過去の演算結果にもとづいてその機能が変換することになる。つまり、自己の出力をフィードバックして機能が決められることになる。

【0043】こういったメモリ機能をつけ加えることにより、更に広範な演算機能を持たせることができる。

【0044】メモリ素子もしくは遅延素子502の出力は図16のように、Aと異なるユニットB(504)の制御入力端子505に入力しても良い。

【0045】(実施例4)図6は本発明の第4の実施例であり、Aの出力が2値カウンタ506に入力されている。Aが1になった回数をカウントし、その回数をバイナリでコード化した3ビットを機能の決定に応用した例である。この場合も勿論他のブロックの機能決定に用いても良いことは言うまでもない。

【0046】以上本発明によれば、回路自身が自分の演算結果に基づいてその構造を変化させたり、新しい機能をつくり出したりできるため、高度情報化社会で必須となる学習、適応、自己増殖といった生命体と類似な柔軟な情報処理を実現することができる。そして、これまでとは全くアルゴリズムやアーキテクチャの異なるコンピュータを実現することができるようになった。

【0047】以上、 $\nu$ MOSインバータのフローティングゲートは常にフローティングの状態で使用する場合のみについて述べたが、これは例えば図18のようにフローティングゲートにスイッチトランジスタ701をつけ、所定の電位 $V_m$ と接続しても良い。あるいはこの電位の値を他のデータとして用いても良い。又、スイッチをコントロールしている信号 $V_s$ は、システムクロックと同期させ毎回フローティングゲート内のチャージを初期状態に戻したりインバータに流れる貫通電流をカットする等の動作をさせても良いことは言うまでもない。

【0048】

【発明の効果】本発明により、学習、適応、自己増殖といった生命体と類似の柔軟な情報処理を可能とする新しい演算処理装置の実現が可能となり、高度な情報処理が可能となる。

【図面の簡単な説明】

【図1】実施例1を説明するブロックダイアグラム。

【図2】4入力Nチャネル $\nu$ MOSトランジスタの概念

図。

【図3】ニューロン回路の一例を示す回路図。

【図4】ニューロン回路の動作を説明するFDP。

【図5】ニューロン回路の一例を示す回路図。

【図6】SHLの一例を示す回路図。

【図7】 $\nu$ MOSインバータ302のFDP。

【図8】第2の実施例を説明するSD数全加算器を示す回路図。

【図9】第2の実施例を説明するSD数全加算器を示す回路図。

【図10】 $\nu$ MOSインバータのFDPを示す図。

【図11】 $\nu$ MOSインバータのFDPを示す図。

【図12】 $\nu$ MOSインバータのFDPを示す図。

【図13】 $\nu$ MOSインバータのFDPを示す図。

【図14】2進SD数の加算を行う回路を示す図。

【図15】第3の実施例を説明するブロック図。

【図16】第3の実施例を説明するブロック図。

【図17】第4の実施例を示すブロック図。

【図18】本発明の他の例を示す回路図。

【符号の説明】

101a, 101b, 101c, 101d 論理演算ユニット、

102a, 102b 入力端子、

103 出力端子、

104a, 104b, 104c, 104d 制御信号入力端子、

105b, 105c 制御入力端子、

201 基板、

202, 203 ソース及びドレイン、

204 ゲート絶縁膜(例えば $\text{SiO}_2$ 膜)、

205 チャネル領域、

206 フローティングゲート電極、

207 絶縁膜、

208a, 208b, 208c, 208d 制御ゲート電極、

210 Nチャネル $\nu$ MOS、

211 Pチャネル $\nu$ MOS、

212  $\nu$ MOSインバータ、

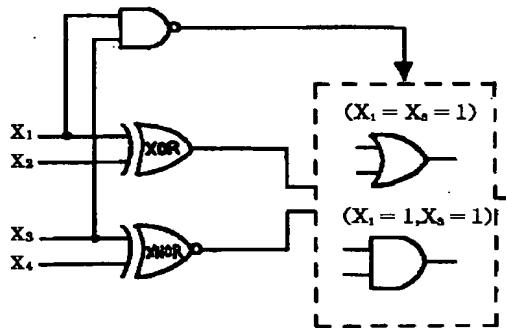
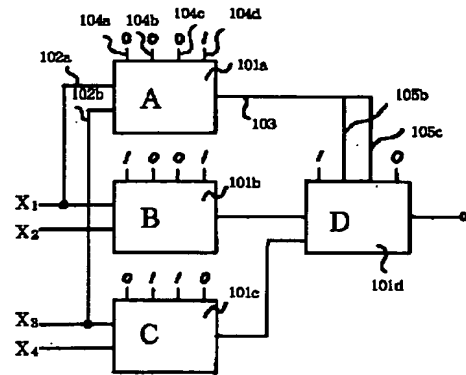
213 通常インバータ、

214 フローティングゲート、

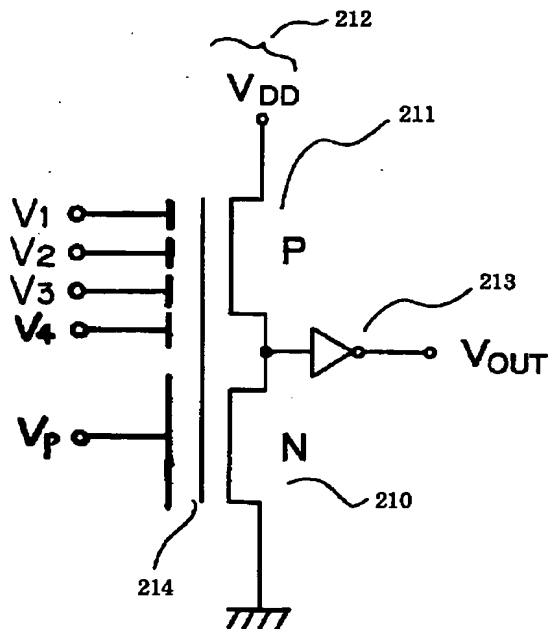
301 D/A変換器、

302, 303, 304, 305, 306  $\nu$ MOSインバータ。

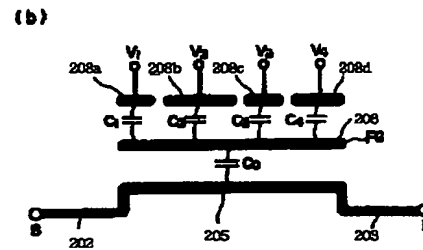
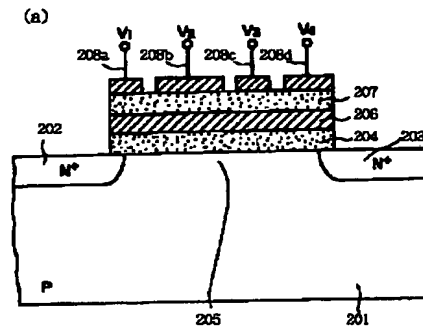
【図1】



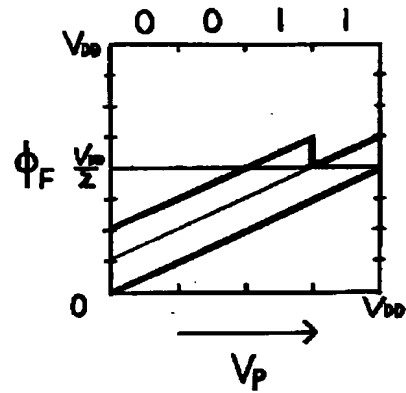
【図3】



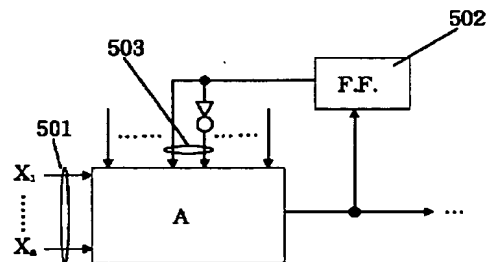
【図2】



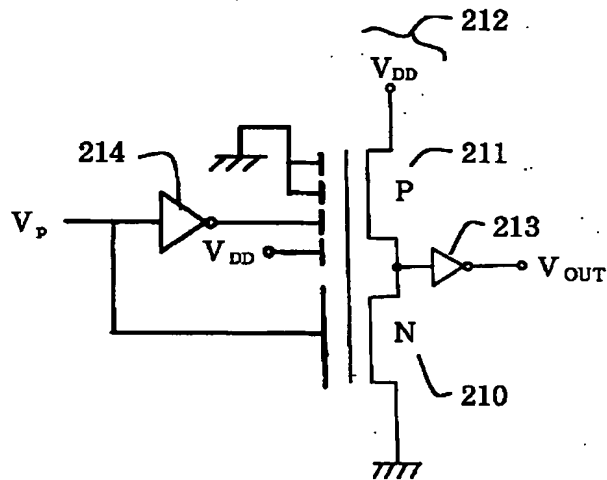
【図4】



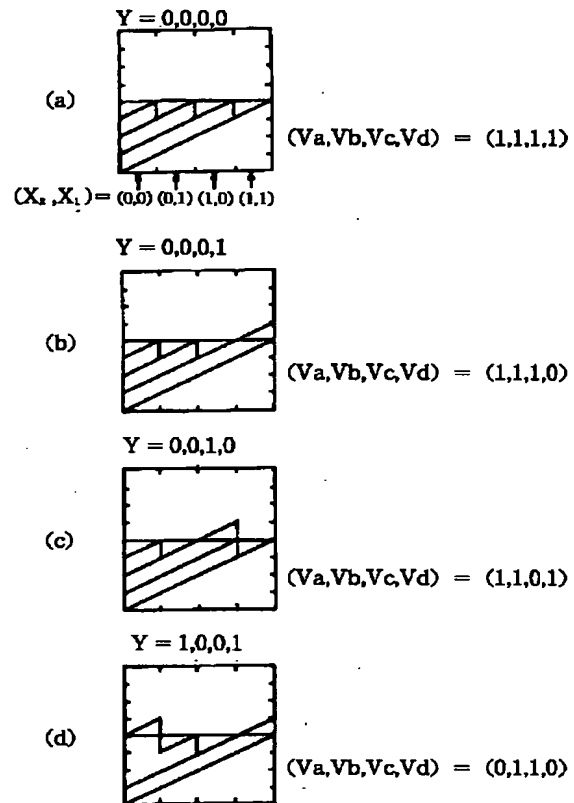
【図15】



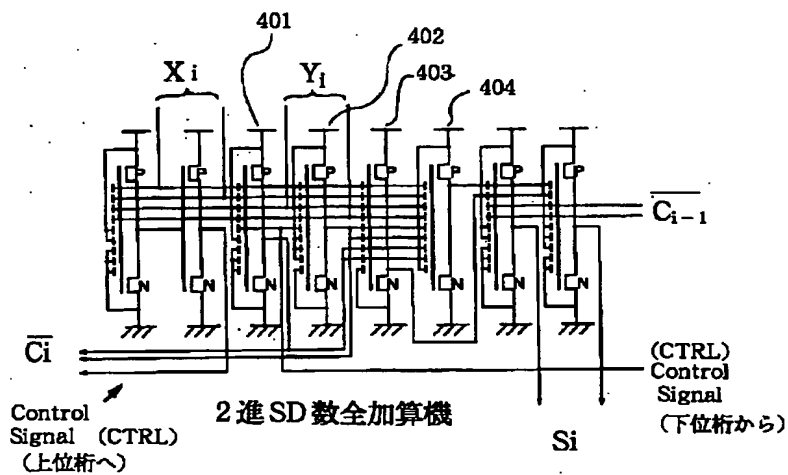
【図5】



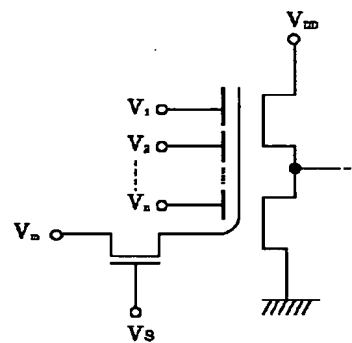
【図7】



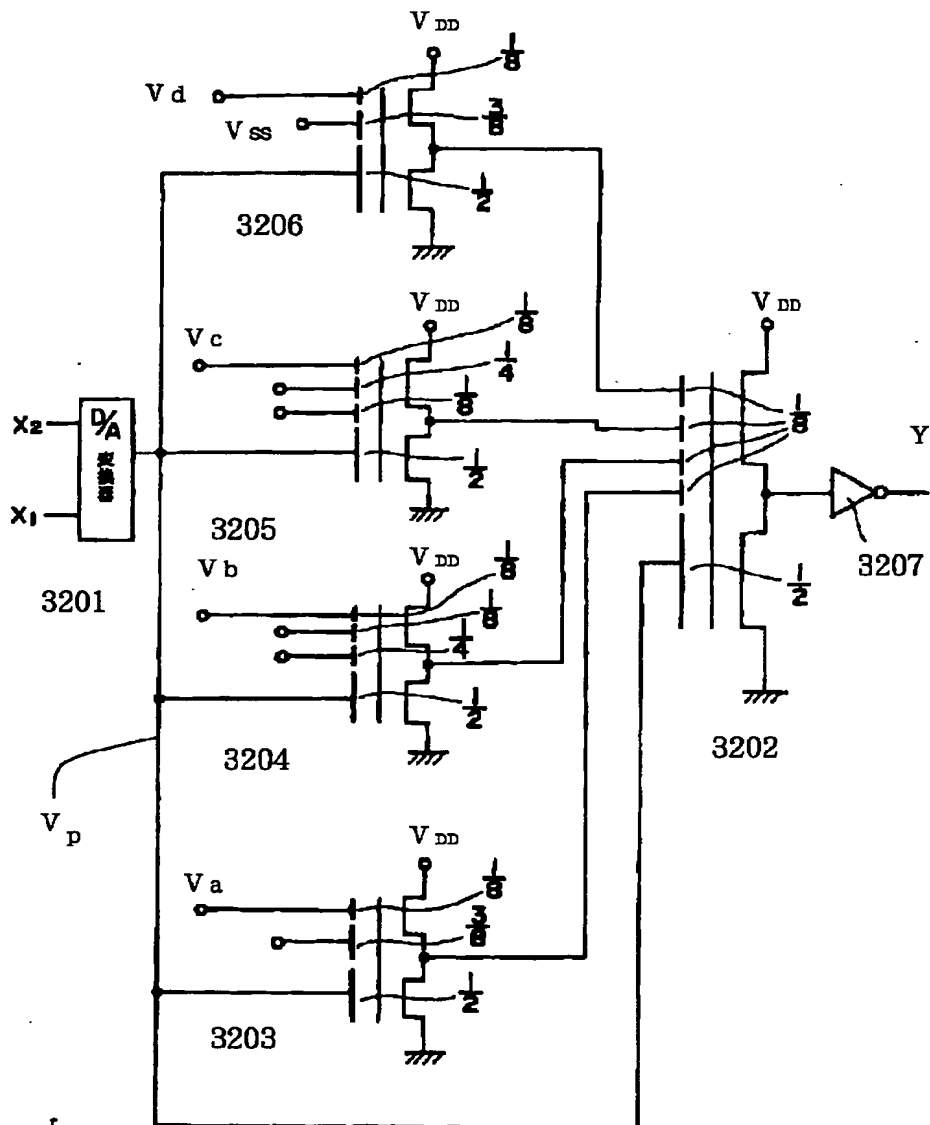
【図8】



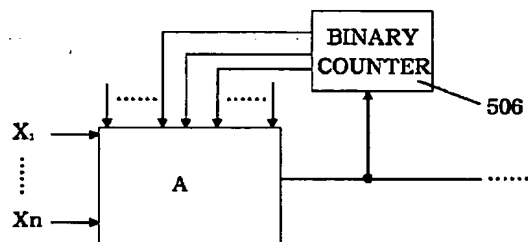
【図18】



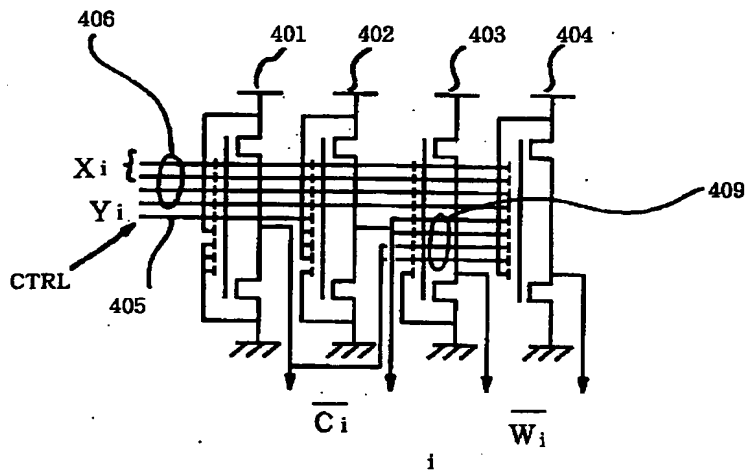
【図6】



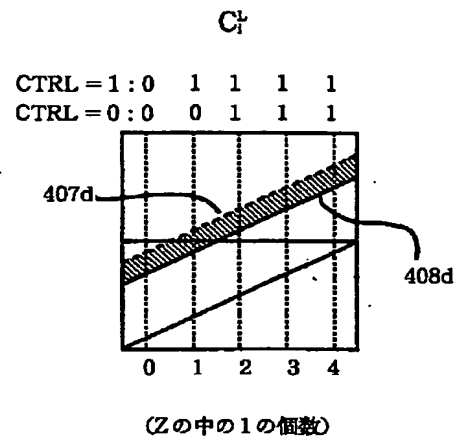
【図17】



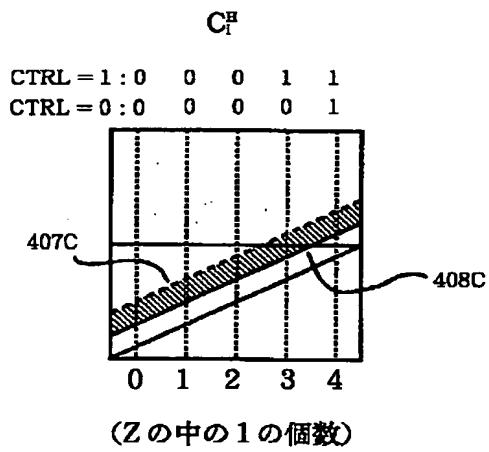
【図9】



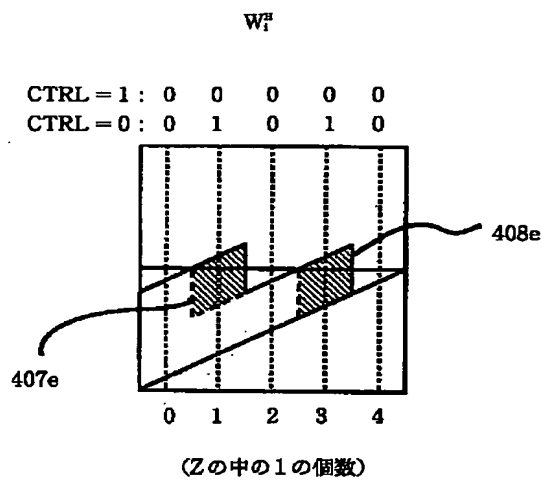
【図11】



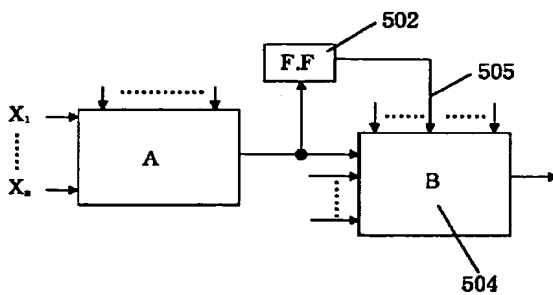
【図10】



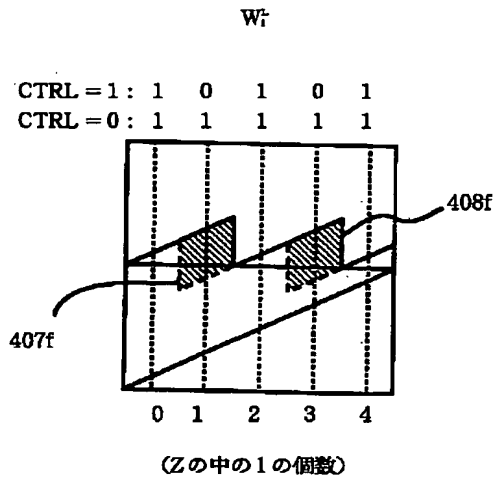
【図12】



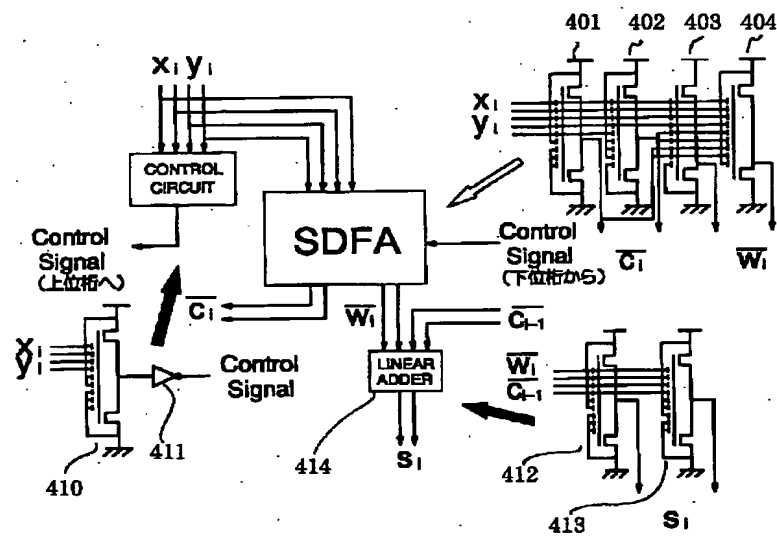
【図16】



【図13】



【図14】



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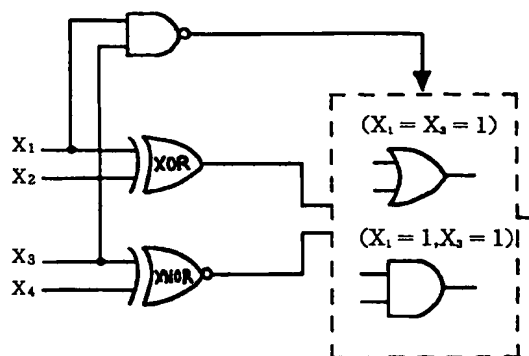
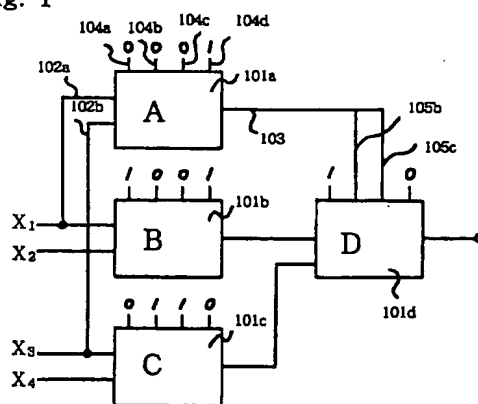
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(54) **COMPUTING DEVICE.**

(57) A novel computing device capable of performing flexible information processing analogous to that of living things, such as learning, adaption, and self-multiplication, which are essential to implement advanced information processing of the future. The device comprises a plurality of first and second input terminals, and a plurality of operational units which execute a given operation of data signals to be inputted into the first input terminals, and each have at least one terminal for outputting the result of the operation. The output signal from one of the output terminals or the result of a given operational processing of this output signal is inputted into at least one of the second input terminals.

**EP 0 685 808 A1**

Fig. 1



## Technical Field

The present invention relates to data processing technology, and in particular, relates to a computing device which makes flexible data processing possible.

## Background Art

Conventionally, the central CPU of computers which conducted data processing technologies comprised semiconductor LSI, and this is termed "hardware". The reason for this is that once the CPU has been constructed, the structure thereof cannot be changed, and it is thus an inflexible structure. Computers can only execute a variety of functions by executing operations in order in the circuits in which these functions are fixed by means of programming. However, in order to realize the high level data processing of the future, it will be necessary to provide data processing such as that conducted by living things, such as learning, adaptation, and self-multiplication such as that performed by human beings; presently, no such computers exist.

There have been a number of attempts to realize flexible data processing by means of software technologies; however, the current state is such that such efforts have met with little success. The reason for this is that hardware, which is inflexible, is used as the base, and even if this is realized in an imitative manner, the burden on the software becomes excessively large, and an enormous amount of time is required even if a supercomputer is employed, so that it is impossible to construct a system which is capable of rapid response.

The so-called "neural networks", which imitate the data processing of the human brain, have been researched and developed as one powerful method for solving such problems; however, these are still far from practical application. The reason for this is that the data processing of the human brain itself is poorly understood, so that the network imitates an extremely primitive structure, and there is no concrete theoretical construction method.

With respect to this, a high performance transistor, termed a "neuron MOS transistor" (inventors: Tadashi Shibata, Tadahiro Ohmi, Japanese Patent Application, Provisional Publication, No. Hei 3-6679) has been invented, and a soft-hardware circuit to which this is applied (inventors: Tadashi Shibata, Tadahiro Ohmi, Japanese Patent Application No. Hei 3-83135) has been invented. In particular, this soft-hardware circuit possesses extremely flexible hardware, the computing functions of which can be freely altered in response to an external signal. When such flexible hardware is employed as the base, there is a possibility of realizing the flexible data processing which was discussed in the opening paragraph; however, a method for this realization has not as yet been made clear.

The present invention has as an object thereof to provide a novel computing device which is capable of forming flexible information processing analogous to that of living things, such as learning, adaptation, and self-multiplication, which are essential to the realization of advanced information processing of the future.

## Brief Description of the Diagrams

Fig. 1 is a block diagram explaining the first embodiment.

Fig. 2 is a conceptual diagram of a 4-input N-channel  $\nu$ MOS transistor.

Fig. 3 is a circuit diagram showing an example of a neuron circuit.

Fig. 4 is an FPD explaining the operation of a neuron circuit.

Fig. 5 is a circuit diagram showing a diagram of a neuron circuit.

Fig. 6 is a circuit diagram showing a diagram of SHL.

Fig. 7 is FPD of a  $\nu$ MOS inverter 302.

Fig. 8 is a circuit diagram of SD number full adder explaining a second embodiment.

Fig. 9 is a circuit diagram showing an SD number full adder explaining the second embodiment.

Fig. 10 shows the FPD of a  $\nu$ MOS inverter.

Fig. 11 shows the FPD of a  $\nu$ MOS inverter.

Fig. 12 shows the FPD of a  $\nu$ MOS inverter.

Fig. 13 shows the FPD of a  $\nu$ MOS inverter.

Fig. 14 shows a circuit which conducts the addition of binary SD numbers.

Fig. 15 is a block diagram for explaining a third embodiment.

Fig. 16 is a block diagram for explaining a third embodiment.

Fig. 17 is a block diagram showing a fourth embodiment.

Fig. 18 is a circuit diagram showing another example of the present invention.

## (Description of the References)

- 101a, 101b, 101c, 101d logical computing units,  
 102a, 102b input terminals,  
 5 103 output terminal  
 104a, 104b, 104c, 104d control signal input terminals,  
 105b, 105c control input terminals,  
 201 substrate,  
 202, 203 source and drain  
 10 204 gate insulating film (for example, SiO<sub>2</sub> film),  
 205 channel region,  
 206 floating gate electrode,  
 207 insulating film,  
 208a, 208b, 208c, 208d control gate electrodes,  
 15 210 N-channel  $\nu$ MOS,  
 211 P-channel  $\nu$ MOS,  
 212  $\nu$ MOS inverter,  
 213 standard inverter,  
 214 floating gate,  
 20 301 D/A converter,  
 302, 303, 304, 305, 306  $\nu$ MOS inverters.

## Disclosure of the Invention

- 25 The computing device in accordance with the present invention is provided with a plurality of first input terminals and a plurality of second input terminals, and a plurality of operational units which execute given operational processing with respect to data signals which are inputted into the first input terminal, by means of control signals inputted into the second input terminals, and which each have at least one output terminal for outputting the results of the operation; characterized in that the output signal from one of the output  
 30 terminals or the result of a given operational processing of this output signal is inputted to at least one of the second input terminals.

## Best Mode for Carrying Out the Invention

- 35 Hereinbelow, embodiments of the present invention will be explained using the diagrams.

## (Embodiment 1)

- 40 Fig. 1(a) is a block diagram showing a first embodiment of the invention. This circuit conducts the following operational processing with respect to 4 digital input signals  $X_1 \sim X_4$ . If  $X_1 = X_3 = 1$ , then when  $X_2 = 0$  or  $X_4 = 1$ , "1" is outputted, and in all other cases, that is to say, in cases in which one or the other of  $X_1$  or  $X_3$  is not equal to 1, a value of "1" is outputted only when  $X_1 \neq X_2$  and  $X_3 = X_4$ .

- The present circuit is comprised by connecting four logical operational units A, B, C, and D (101a ~ 101d) to one another by means of wiring. Each operational unit is provided with two input terminals (102a, 102b, and the like), one output terminal 103, and four control signal input terminals (104a, 104b, 104c, 104d, and the like), and the operational functions are stipulated by means of a signal having a value of 0 or 1 which is inputted into the control input terminals. A value of 0 indicates that 0V and a value of 1 indicates that the power source voltage  $V_{DD}$  (5V), respectively, are applied to the input terminals. In such a circuit, soft-hardware logical circuits (Japanese Patent Application No. Hei 3-83135) using, for example, neuron  
 50 MOS transistors (Japanese Patent Application, Provisional Publication, No. Hei 3-6679) may be employed. The neuron MOS transistor and the soft-hardware logical circuit are separately explained.

- The blocks A, B, and C become, respectively, NAND circuits, XOR circuits, and XNOR circuits, in response to the input signals into the control input terminals (104a ~ 104d) which are shown in the figure. In the case of block D, the two control input terminals 105b and 105c have the outputs of block A (NAND circuit) inputted thereinto rather than fixed signals, so that if the output 103 has a value of 0, this block  
 55 becomes an OR circuit, while if the value is 1, the block becomes an AND circuit. These relationships are depicted in a simplified form in Fig. 1(b).

The portion corresponding to block D has functions which differ depending on the results of the NAND operation of  $X_1$  and  $X_3$ .

As shown above, in the present embodiment, the circuit executes a flexible operational function by means of altering the functions of a portion of a circuit or altering the functions of the entirety of the circuit by means of the operational results.

In the foregoing, an extremely simplified case was shown, so that the importance of this novel flexible function may not be clear; however, this will be discussed in detail in the second embodiment, after the explanation of the neuron MOS transistor and the soft-hardware logical circuit using, respectively, Figs. 2 ~ 7.

First, the structure and operational principle of the neuron MOS transistor (hereinbelow abbreviated to "νMOS") will be explained. Fig. 2 shows an example of the cross sectional structure of a 4-input N-channel νMOS transistor; reference 201 indicates, for example, a P-type silicon substrate, references 202 and 203 indicate a source and drain formed from  $N^+$  diffusion layers, reference 204 indicates a gate insulating film (for example,  $SiO_2$  film) which is provided on channel region 205 between the source and the drain, reference 206 indicates a floating gate electrode which is electrically insulated and is in a potentially floating state; reference 207 indicates an insulating film comprising, for example,  $SiO_2$ , and references 208a, 208b, 208c, and 208d indicate control gate electrodes. Fig. 2(b) shows a further simplified version of this for the purposes of analyzing the operation of the νMOS. If the capacitive coupling coefficients between each control gate electrode and the floating gate are represented by  $C_1$ ,  $C_2$ ,  $C_3$ , and  $C_4$ , as in the figure, and the capacitive coupling coefficient between the floating gate and the silicon substrate is represented by  $C_0$ , then the potential  $\Phi_F$  of the floating gate is given by the following formulas.

$$\Phi_F = (1/C_{TOT}) (C_1 V_1 + C_2 V_2 + C_3 V_3 + C_4 V_4) \quad (1)$$

$$\text{Here, } C_{TOT} = C_0 + C_1 + C_2 + C_3 + C_4 \quad (2)$$

$V_1$ ,  $V_2$ ,  $V_3$ , and  $V_4$  indicate voltages which are applied to, respectively, input gates 208a, 208b, 208c, and 208d, and the potential of the silicon substrate is 0V, so that it is grounded.

Now, the potential of source 202 is set to 0V. That is to say, it is set to a value in which the potentials of all the electrodes are measured using the source as a standard. In this way, if the floating gate 206 is seen as a standard gate electrode, the νMOS shown in Fig. 2 becomes equivalent to a standard N-channel MOS transistor, and when the gate potential  $\Phi_F$  thereof exceeds a threshold value ( $V_{TH}$ ), the source and the drain become electrically connected. That is to say, from formula (1), the νMOS becomes conductive (enters an ON state) when the following conditions are met.

$$(C_{TOT}) (C_1 V_1 + C_2 V_2 + C_3 V_3 + C_4 V_4) > V_{TH} \quad (3)$$

The foregoing explanation referred to an N-channel MOS transistor; however, there are devices having the structure shown in Fig. 2(a) in which the source 202, the drain 203, and the substrate 201 are all of the opposite conductivity type. That is to say, such a νMOS has an N-type substrate, and the source and drain are formed from  $P^+$  diffusion layers, and this is termed a "P-channel MOS transistor".

#### Neuron Circuit, Soft-Hardware Logical Circuit

Next, the most fundamental circuit used in the νMOS, the neuron circuit, and the operation thereof will be explained using Fig. 3. The neuron circuit comprises a νMOS inverter 212, comprising a N-channel νMOS 210 and a P-channel νMOS 211, and a standard inverter 213. This circuit is such that the νMOS inverter inverts when the potential  $\Phi_F$  of the common floating gate 214 exceeds the inversion voltage  $(1/2) V_{DD}$  of the νMOS inverter, and  $V_{OUT}$  becomes "1". In the figure, the capacitive coupling coefficients of the  $V_1 \sim V_4$  gates are all set to  $(1/8) C_{TOT}$ , and the capacitive coupling coefficient of the  $V_P$  gate is set to  $(1/2) C_{TOT}$ , and for the purposes of simplicity, it is assumed that  $C_0 = 0$ . The  $V_P$  gate is termed the "main electrode" of the νMOS inverter.

It is possible to analyze the operation of this circuit in a simple manner by means of the floating gate potential diagram (abbreviated to "FPD") shown in Fig. 4. the FPD depicts  $\Phi_F$  as a function of  $V_P$ , and if  $V_1 \sim V_4 = 0$ , then when  $V_P$  changes from 0 to  $V_{DD}$ ,  $\Phi_F$  changes from 0 to  $(1/2) V_{DD}$ . This is because the coupling capacity of  $V_P$  is  $(1/2) C_{TOT}$ . That is to say, the potential of the neuron circuit is constantly 0.

In the example shown in Fig. 4,  $V_1 = V_2 = 0$ ,  $V_4 = V_{DD}$ , and  $V_3$  has a value of  $V_{DD}$  when  $V_P$  is within a range of  $0 \sim (3/4) V_{DD}$ , and a value of 0 when  $V_P > (3/4) V_{DD}$ . In this way,  $\Phi_F$  is such that a value of  $V_{OUT}$  of 1 is outputted when  $V_P > (1/2) V_{DD}$ . In order to realize such a circuit, as shown in Fig. 5,  $V_P$  may be passed

through a pre-inverter 214 having a threshold value of  $(3/4) V_{DD}$  before being inputted into  $V_3$ . Such circuits are the basis of the soft-hardware logic circuits (abbreviated to "SHL").

Next, an example of an SHL circuit will be explained using Figs. 6 and 7. In Fig. 6, a circuit diagram is shown. Reference 301 indicates a D/A converter which is provided at the input stage; this generates a 4-level multivalent variable  $V_p$  with respect to combinations of two inputs  $X_1$  and  $X_2$ .  $V_p$  is inputted into the main gate of the 5  $\mu$ MOS inverters 302 ~ 306. The relationships between  $X_1$  and  $X_2$  and  $V_p$  are shown on the horizontal axis of the FPDs shown in Fig. 7(a).  $V_a$ ,  $V_b$ ,  $V_c$ , and  $V_d$  correspond to, for example, the control signal input terminals 104a ~ 104d of the operational block A of Fig. 1. In the figure, the fractions such as  $1/2$ ,  $1/4$ ,  $1/8$ , and the like, indicate the capacitive coupling coefficients between the respective input gates and the floating gate, and these indicate, respectively,  $(1/2) C_{TOT}$ ,  $(1/4) C_{TOT}$ ,  $(1/8) C_{TOT}$ , and the like.

In the present circuit, signals having the two values of 0 or  $V_{DD}$  are inputted into  $V_a$ ,  $V_b$ ,  $V_c$ , and  $V_d$ . The case in which  $V_a = V_b = V_c = V_d = 1 (= V_{DD})$  is shown in the FPD of  $\mu$ MOS inverter 302 which is shown in Fig. 7(a). The FPDs of  $V_a$ ,  $V_b$ ,  $V_c$ , and  $V_d$  relating to other combinations, and examples of outputs are shown in Fig. 7(a), (b), (c), and (d). It can be seen that the inversion signals of the signals inputted into  $V_a$ ,  $V_b$ ,  $V_c$ , and  $V_d$  are outputted in response to  $(X_2, X_1) = (0, 0)$ ,  $(0, 1)$ ,  $(1, 0)$ , and  $(1, 1)$ . It is possible to designate the output pattern and to determine the form of the function directly by means of  $V_a$  ~  $V_d$ , so that the determination of the function can be easily conducted, and this is a major characteristic feature.

The circuit shown in Fig. 6 is only an example of an SHL, and it is of course the case that it is possible to use other SHLs which are described in the patent specification (Japanese Patent Application No. Hei 3-83135).

#### (Embodiment 2)

Next, a second embodiment of the present invention is shown in Fig. 8. This is a computing circuit which employs one  $\mu$ MOS inverter as an operating block and comprises 8 such blocks; it is a binary SD number adder. Conventionally, when conducting addition operations, addition was conducted starting with the least significant bit, carrying the result after each calculation, and proceeding to the next bit, so that when the bit length was long, there was an operational period delay in proportion to this. This constituted a great hindrance to high-speed operational processing.

The present embodiment realizes an adder in which the carry over only affects the immediately following place, so that there is no so-called "carry over propagation"; this is realized in a simple manner for the first time by using SHL circuits, and altering the functions of a portion of the circuit blocks using a portion of the operational results. Prior to the explanation of the present embodiment, the SD numerical system will be explained.

The Signed-Digit (SD) numerical system [1] is a numerical system which expresses signals having a plurality of values. What is meant by an "SD numerical system" is a method of expression having a large expressive capacity; for this reason, it has superior characteristic features. For example, in an SD number adder, the carry propagation is limited to one stage irrespective of word length, so that operations proceed essentially in parallel. If this characteristic feature is taken advantage of, high speed operation becomes possible.

What is meant by a "binary SD number" is the number  $X$  which is defined as shown below.

$$X = a_{n-1} 2^{n-1} + a_{n-2} 2^{n-2} + \dots + a_1 2 + a_0$$

$$a_i \in \{-1, 0, 1\}$$

That is to say, in this numerical system, one place (one bit) can have 3 values; however, this is a binary number, not a base 3 number. That is to say, the numerical system has a larger expressive capacity. For example,  $(1, -1, 0)$  and  $(0, 1, 0)$  can be expressed by the same binary SD number. Consideration will now be given to the addition of SD numbers. The  $i$ -place of 2 binary SD numbers will be represented by  $x_i$  and  $y_i$ , and the linear sum thereof is represented by  $z_i$ .

$$x_i \in \{-1, 0, 1\}$$

$$y_i \in \{-1, 0, 1\}$$

$$z_i = x_i + y_i \in \{-2, -1, 0, 1, 2\}$$

With respect to this  $z_i$ , a carry  $c_i$  and an intermediate sum  $w_i$  in accordance with the following formula:

$$z_i = 2c_i + w_i$$

$$c_i, w_i \in \{-1, 0, 1\}$$

are determined; however, at this time, the carry and intermediate sum may be determined under the conditions shown in Table 1 in consideration of the linear sum  $z_{i-1}$  of the less significant bit.

Table 1

Table of the true values of the carry c and the intermediate sum w of an SD adder.			
$z_i$	$z_{i-1}$	$c_i$	$w_i$
2	*	1	0
1	$\geq 0$	1	-1
	$< 0$	0	1
0	*	0	0
-1	$< 0$	-1	1
	$\geq 0$	0	-1
-2	*	-1	0

If the intermediate sum  $w_i$  and the carry  $c_{i-1}$  obtained from the less significant bit which are obtained here are added in a linear manner, the final sum  $s_i$  is obtained. During the determination of the conditions described above, a carry is generated in consideration of the linear sum of the less significant bit, so that there is no carry over generated in the calculation which obtains the final sum. Accordingly, carry propagation is limited to the adjacent bit. The foregoing is the SD numerical additional algorithm.

In order to realize this algorithm using  $\nu$ MOS, first, binary SD numbers having 3 values were coded into 2-bit binary numbers. This is because when a  $\nu$ MOS inverter is employed, the output of the inverter has two values. Tables 2 and 3 show coding tables.

Table 2

Coding of binary SD numbers and 2-bit binary numbers		
Binary SD	Binary Number	
1	1	1
0	0	1
-1	0	0

Table 3

Coding of the linear sum w	
z	x + y
2	Four 1's
1	Three 1's
0	Two 1's
-1	One 1
-2	One 1

When transforming SD numbers having three values into 2-bit binary numbers, coding was conducted focusing on the number of 1's. With respect to z, which is the linear sum of x and y, this was coded by one number contained between x and y. The true value table of the SD addition described above is rewritten in

accordance with this coding. Furthermore, the true value table divided into two based on whether  $z_{i-1}$ , which is the linear sum of the less significant place, is greater than or equal to 0, or less than 0.

The rewritten true value table is shown in Table 4.

Table 4

True value table rewritten for vMOS logic circuits

(a) Control signal is "1"

(b) Control signal is "0"

( $z_{i-1} \geq 0$ )

$z_i$	$C_i$		$w_i$	
Four 1's	1	1	0	1
Three 1's	1	1	0	0
Two 1's	0	1	0	1
One 1	0	1	0	0
Zero 1	0	0	0	1

( $z_{i-1} < 0$ )

$z_i$	$C_i$		$w_i$	
Four 1's	1	1	0	1
Three 1's	0	1	1	1
Two 1's	0	1	0	1
One 1	0	0	1	1
Zero 1	0	0	0	1

Here, what is meant by the "control signal" is a variable which takes a value of "1" when the linear sum  $z_{i-1}$  of the less significant bit is "0" or more, and takes a value of "0" when this sum is less than "0". With respect to  $c_i$  and  $w_i$  in the true value table, the left-hand column divided by a dotted line represents the more significant bit, while the right hand column represents the less significant bit.

The circuit diagram of Fig. 9 shows a realization of the true value table shown in Table 4 using vMOS logic circuits. This figure depicts the circuit blocks 401 ~ 404 of Fig. 8; the circuit outputs the inverted signals of carry  $C_i$  and the sum  $W_i$ , respectively, of  $X_i$  and  $Y_i$ .

A symmetrical function vMOS logic circuit having a total of 4-bit inputs, the two bits of input  $x$  and the two bits of input  $y$ , is employed. The number of 1's, which is the result of the coding of  $z$ , is employed in an unchanged manner as the main variable  $V_p$  of the vMOS inverter. Figs. 10, 11, 12, and 13 show FPDs of vMOS inverters 401 ~ 404, in which the number of 1's within  $Z$  is depicted as the main variable  $V_p$ .

For example, in the vMOS inverter which calculates the more significant bit of carry  $c$  (Fig. 10), when the control signal CTRL is "0", "00001" is set as the target function (the output characteristics), and when the control function is "1", the target function is set to "00011". That is to say, the input terminal 405 of the control signal CTRL functions as a control signal input terminal which controls the operating function of operational blocks 401 and 402. The terminal 406 into which  $x_i$  and  $y_i$  are inputted is a data signal input terminal. In Figs. 10 ~ 13, the form of the function when CTRL = 1 is shown by the dotted line and the shaded area (407c ~ f), while the form of the function when a CTRL = 0 is shown by the solid line (408c ~ f).

In this way, the SD number adder (SDFA) circuit shown in Fig. 9 is realized. In order to simplify the circuit, carry  $c$  and intermediate sum  $w$  are outputted as inverted values. The vMOS inverter which calculates the more significant bit of the carry described above is the left-most inverter 401. Here, consideration will be given to the vMOS inverter 403 which calculates the more significant bit of the intermediate sum  $w$ . When the control signal is "0", the target function of this neuron circuit is "01010". This is an XOR function. When the control signal is "1", the target function is "00000". In this way, in order to calculate the more significant bit of the intermediate sum  $w$ , this vMOS inverter operating unit has a function which is changed when an XOR function is calculated by means of the control signal CTRL, or when, irrespective of input, a value of "0" is outputted. Here, the output of vMOS inverters 401 and 402 which calculate the carry is inputted into the control signal input terminal 409 which determines the function of operating units 403 and 404, and the function thereof can be changed where necessary. By means of this, the calculation of the intermediate sum is realized.

Fig. 14 shows all the circuitry corresponding to one decimal place which conducts the addition of the binary SD numbers. The control signal CTRL is produced by means of a control circuit comprising one  $\mu$ MOS inverter (410) and one standard inverter (411). Furthermore, s, which represents the final addition result, is obtained by conducting the addition of the intermediate sum w and the carry from the less significant place by means of a linear adder 414, comprising 2  $\mu$ MOS inverters 412 and 413.

In the above manner, a binary SD number adder can be constructed in an extremely simple manner by means of the present invention. The number of transistors required is only 16 per decimal place, and this was heretofore not realizable by means of such simple circuitry.

The binary SD number adder described above is a circuit which outputs signals in which binary SD numbers are coded in 2-bit binary numbers. If the binary SD numbers are expressed as positive voltage values, these can be directly coupled to the floating gate of the  $\mu$ MOS inverter as signals having three values. Furthermore, the output may be outputted after converting the 2-bit binary output to a three-value SD number at the  $\mu$ MOS source follower circuit. That is to say, the SD adder described in the present embodiment is a circuit which is capable of easy interface with binary signals and signals having a plurality of values, so that it has an extremely broad range of applications.

#### (Embodiment 3)

A third embodiment of the present invention is shown in Fig. 15. Here, a representative example employing an operating unit A having a number n of input terminals for data signals is shown. The output of unit A is applied to flip-flop 502, and the output thereof is again applied to the portion 503 of the control input terminal which determines the function of the unit A itself. This flip-flop may also be a shift register which is controlled by means of a clock. When the output of A has a predetermined delay applied thereto and is then inputted into the control input terminal in this manner, the function thereof changes based on the past operation results. That is to say, the output of the unit itself is subjected to feedback and determines the function thereof. By means of adding this type of memory function, it is possible to provide an even wider range of operating functions.

The output of the memory element or a delay element 502 may be inputted into the control input terminal 505 of a unit B (504) different from the unit A, in the manner shown in Fig. 16.

#### (Embodiment 4)

Fig. 6 shows a fourth embodiment of the present invention; the output of A is inputted into a binary counter 506. This is an example in which the number of times A has a value of "1" is counted, and the three bits into which this number is encoded in a binary fashion are applied to the determination of the function. It is of course the case that in this case as well, this may be used in order to determine the function of other blocks.

In accordance with the present invention described above, the circuit itself may change structure or produce new functions based on its own operational results, so that it is possible to realize flexible information processing analogous to that of living things, such as learning, adaptation, and self-multiplication, which are necessary in a society dealing with a high level of information. Additionally, it is possible to realize computers having completely different algorithms and architecture from those which have previously existed.

In the foregoing, only that case was shown in which the floating gate of the  $\mu$ MOS inverter was in a constantly floating state; however, as shown in Fig. 18, a switch transistor 701 may be added to the floating gate, and a given voltage  $V_m$  may be connected. Alternatively, the value of this potential may be employed as other data. Furthermore, the signal  $V_s$  which controls the switch may of course be synchronized with a system clock, and the charge within the floating gate may be returned to the original state each time, or the current flowing to the inverter may be cut, or the like.

#### Industrial Applicability

By means of the present invention, it is possible to realize a novel computing and processing device which is capable of flexible information processing analogous to that of living things, such as learning, adaptation, and self-multiplication, and high level information processing is possible.

**Claims**

1. A computing device, comprising a plurality of first input terminals and a plurality of second input terminals, and a plurality of operational units which execute given operations, stipulated by means of control signals inputted into said second input terminals, with respect to data signals inputted into said first input terminals, and which each have at least one output terminal for outputting results thereof; characterized in that the output signal outputted from one of said output terminals or the result of a given operational processing of this output signal, is inputted into at least one of said second input terminals.
2. A computing device in accordance with Claim 1, characterized in that said operational units contain inverters comprising at least one stage of neuron MOS transistors.

Fig. 1

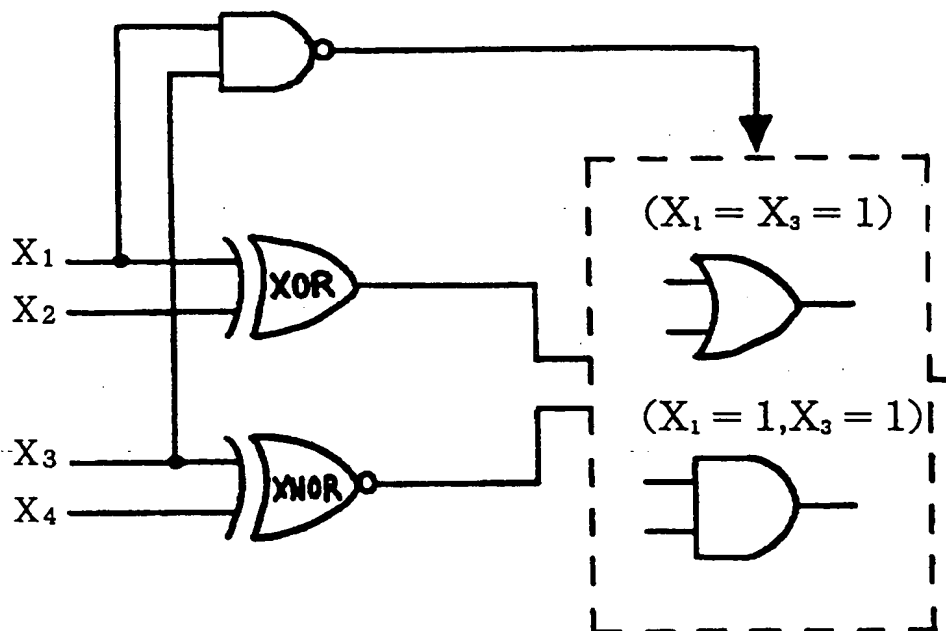
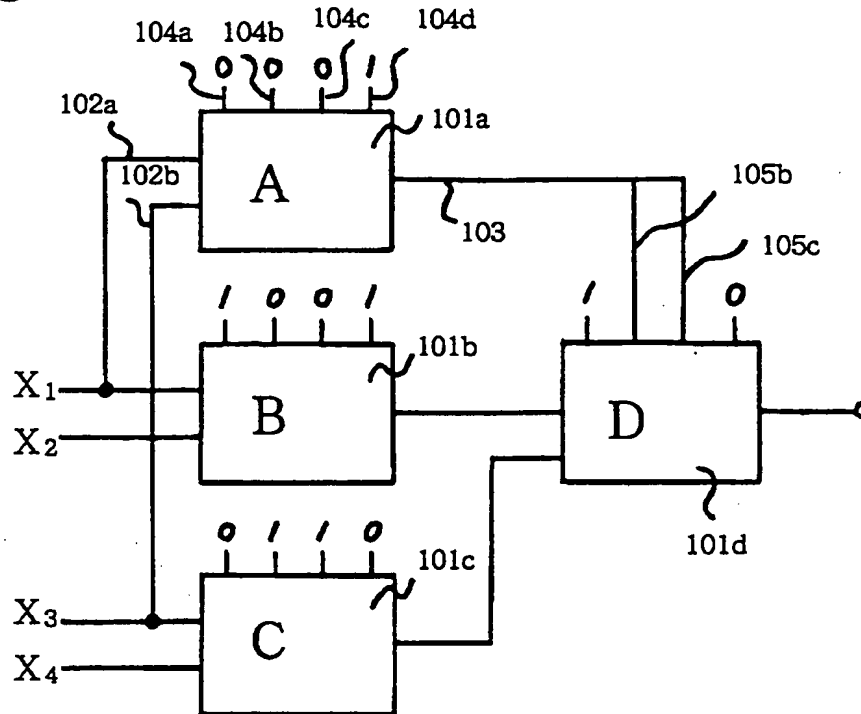


Fig. 2 (a)

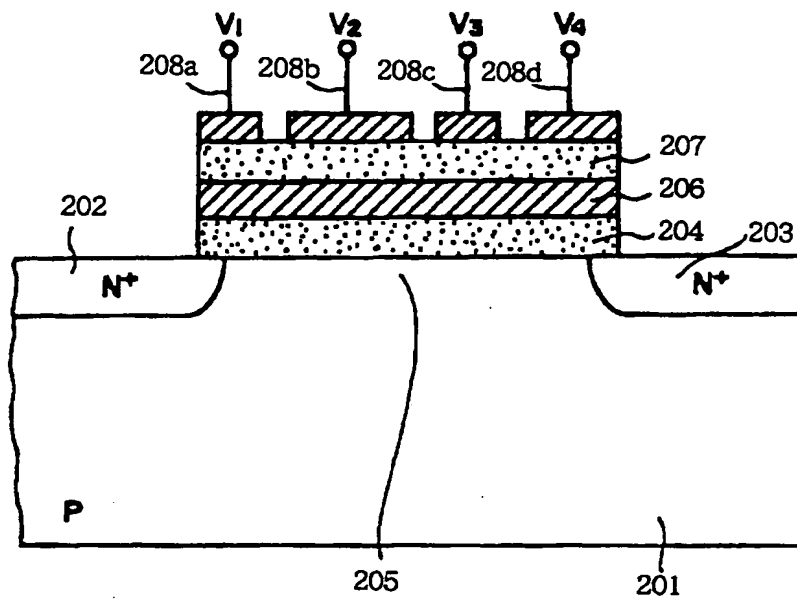


Fig. 2 (b)

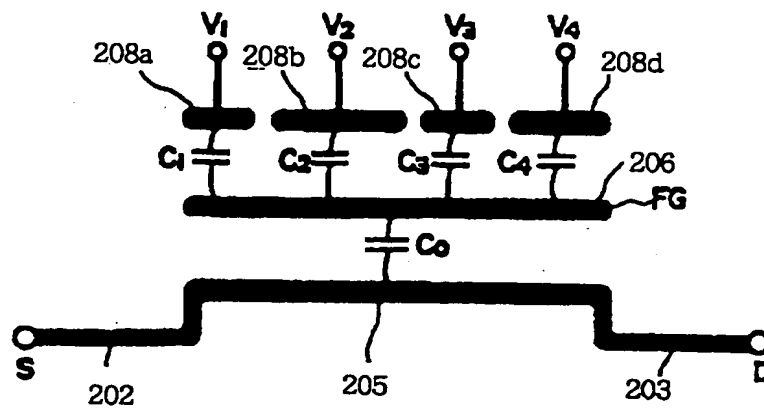


Fig. 3

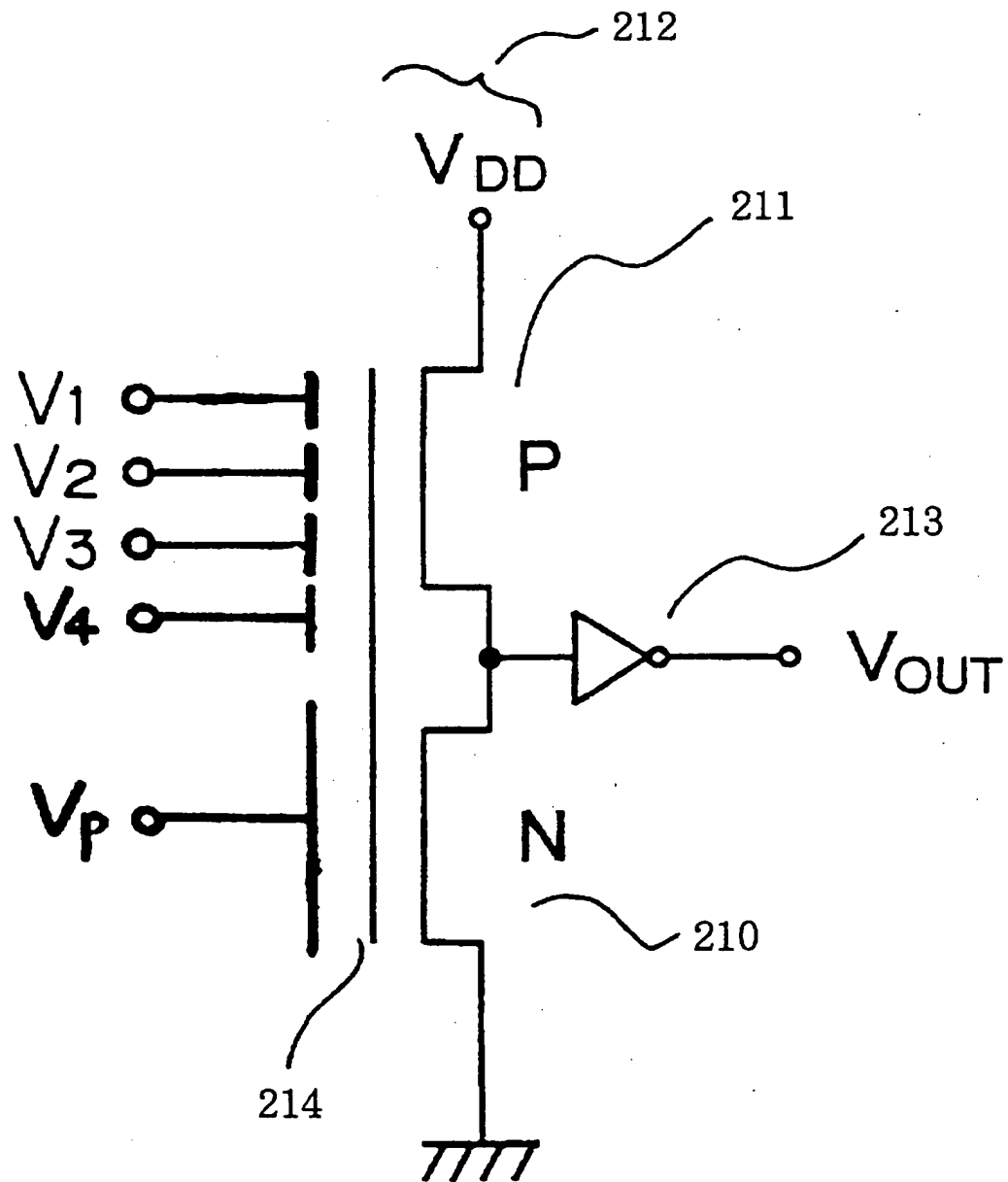


Fig. 4

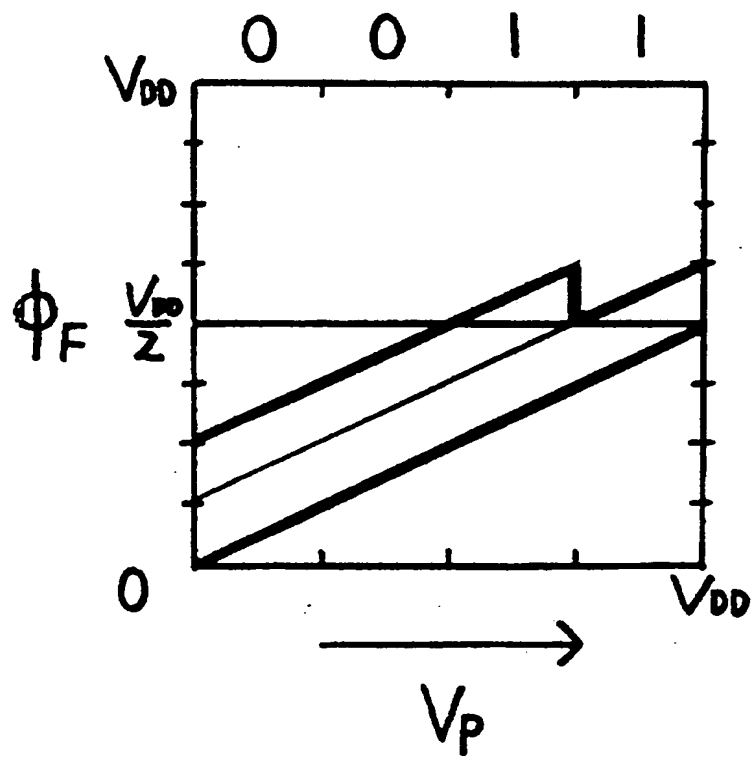


Fig. 5

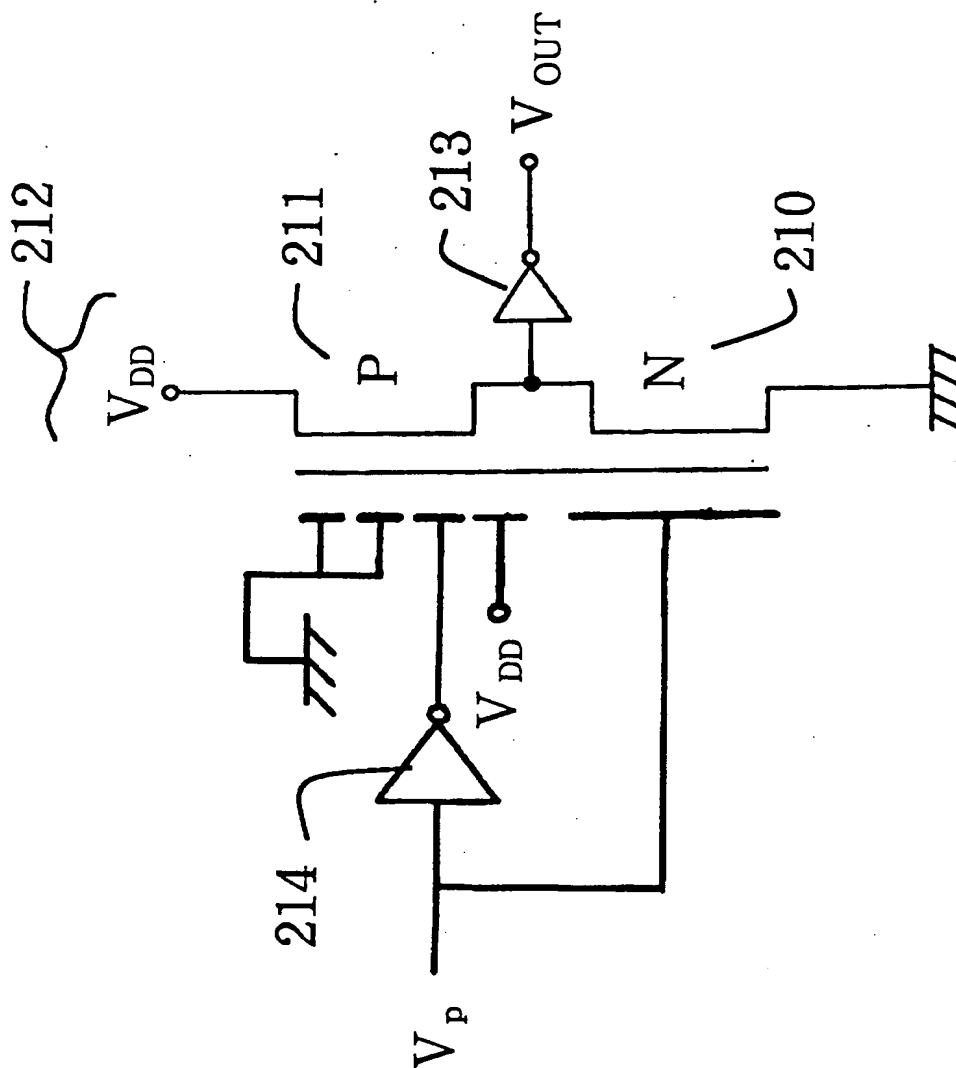
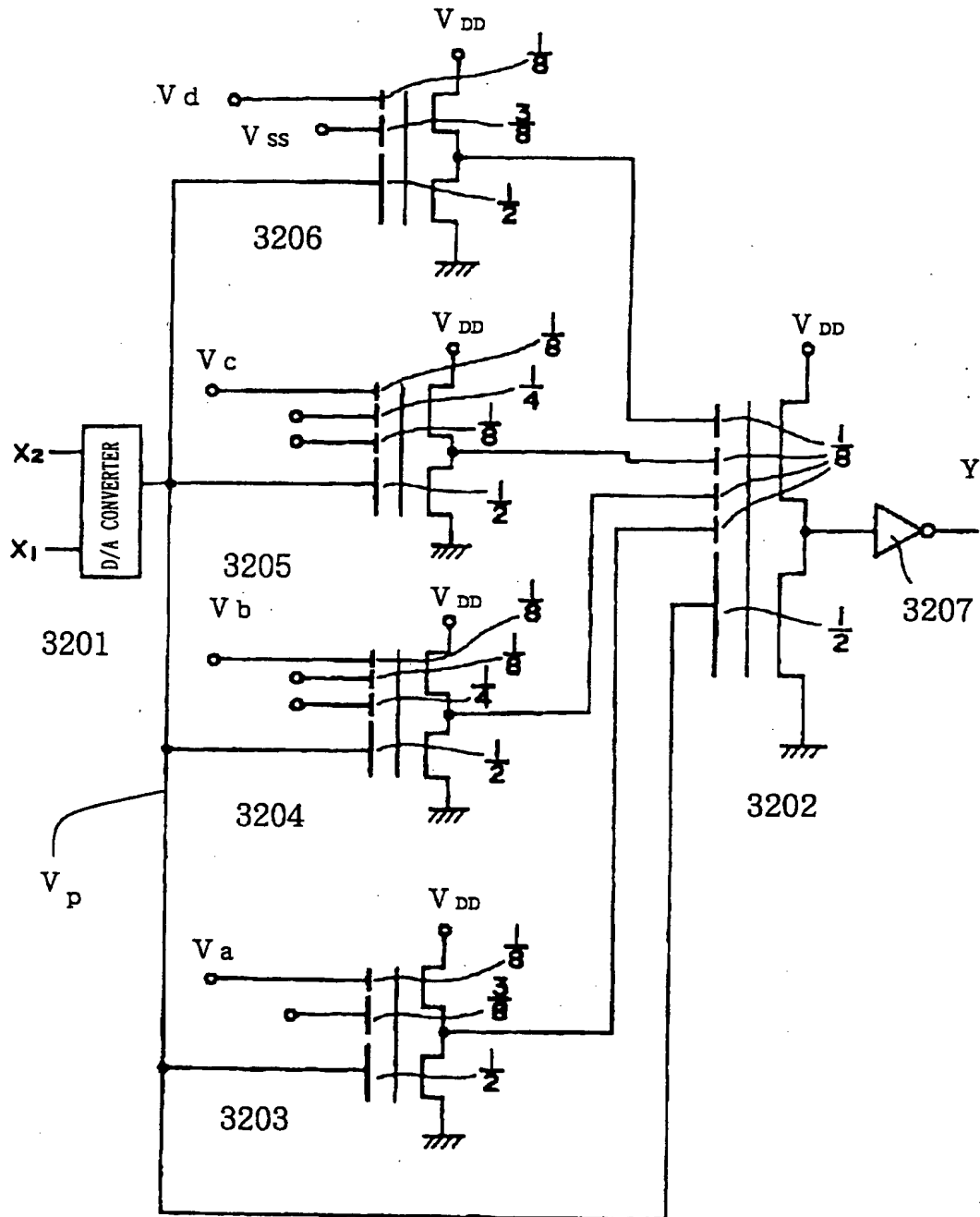


Fig. 6



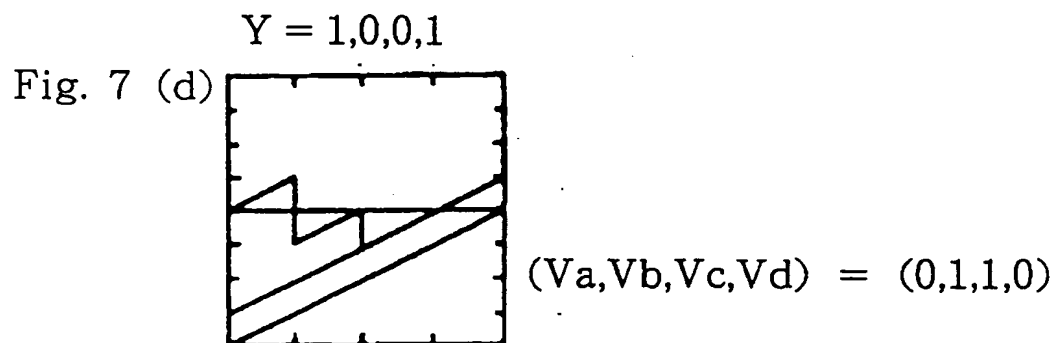
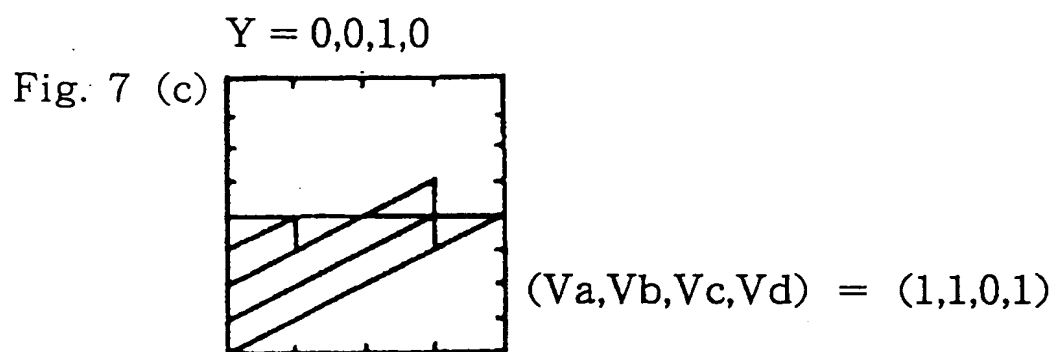
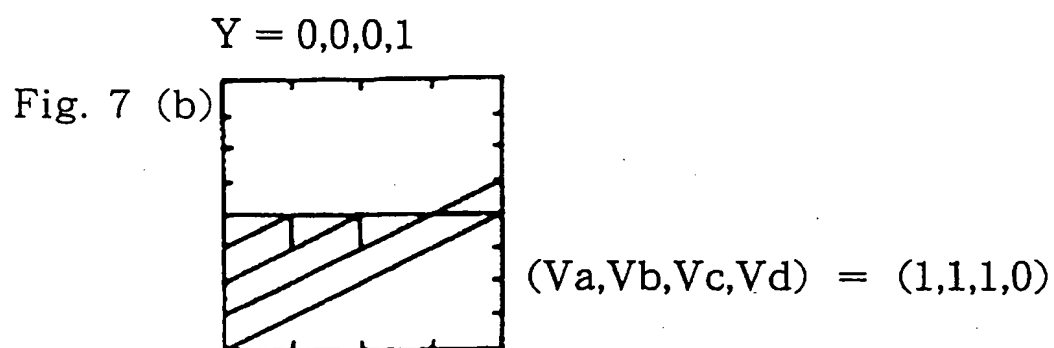
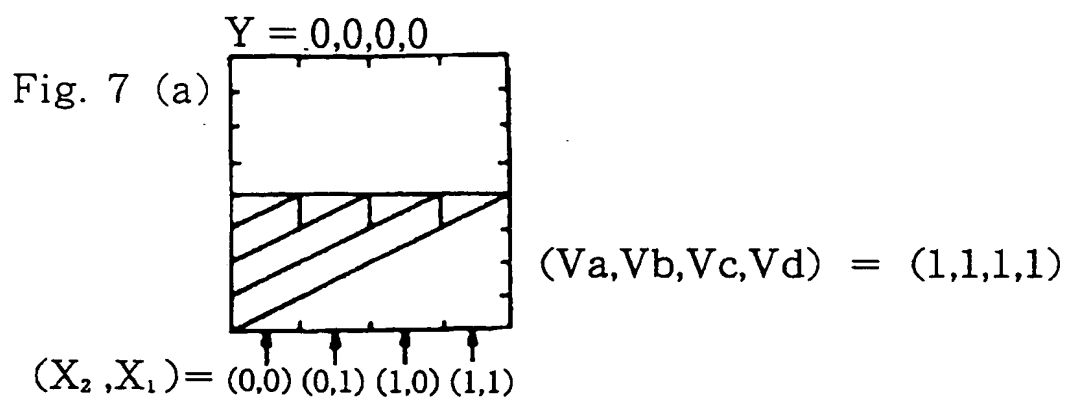


Fig. 8

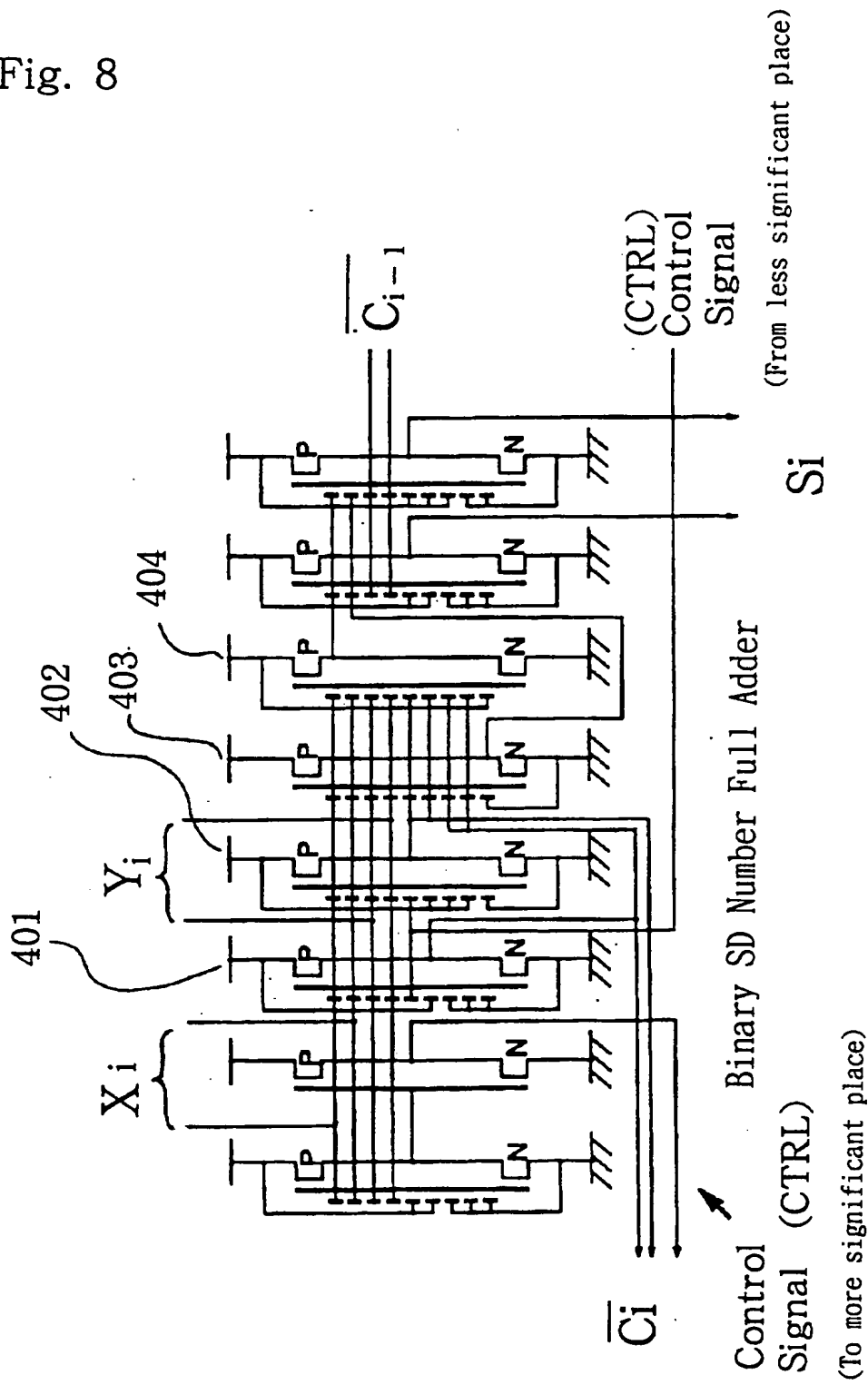


Fig. 9

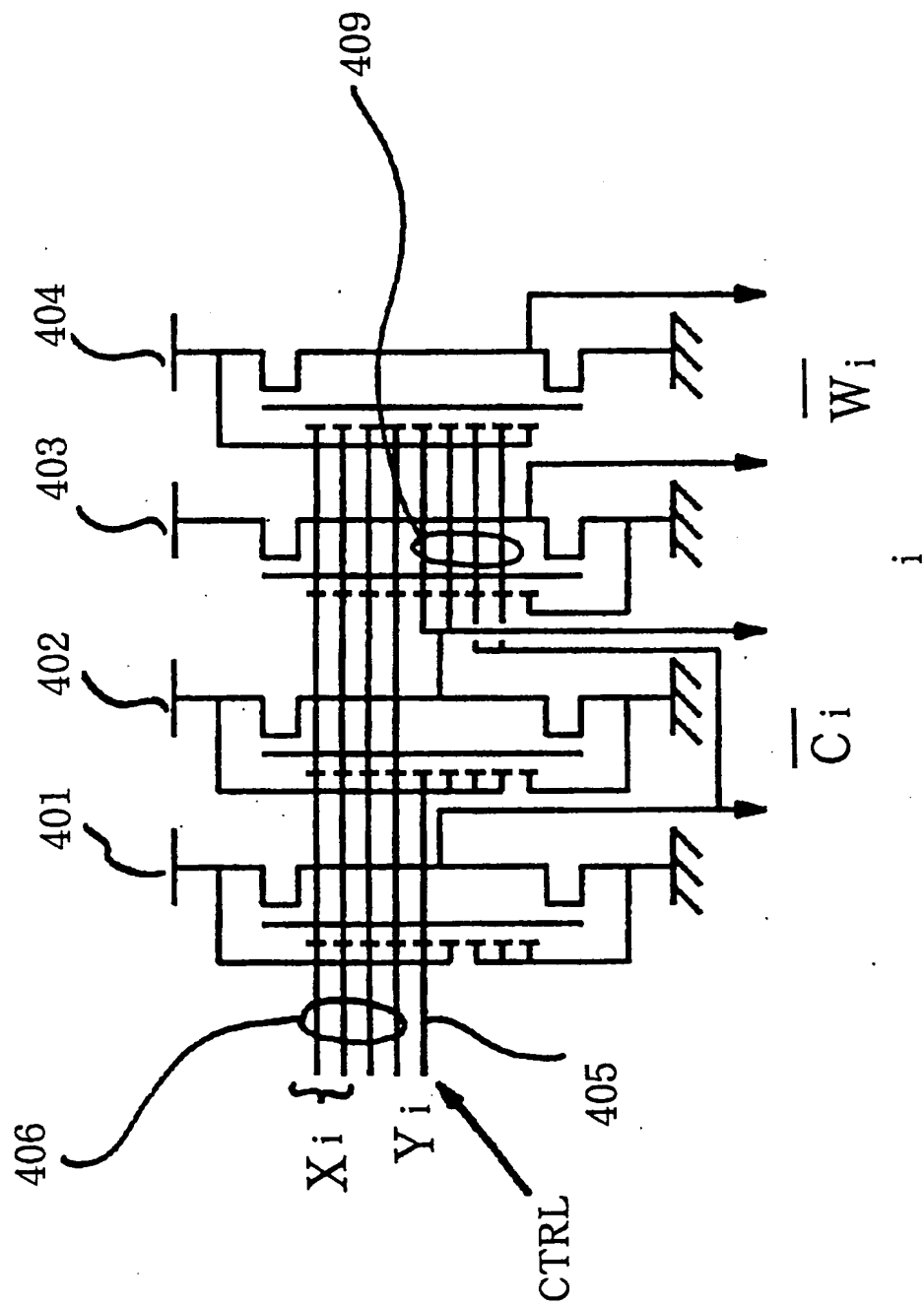


Fig. 10

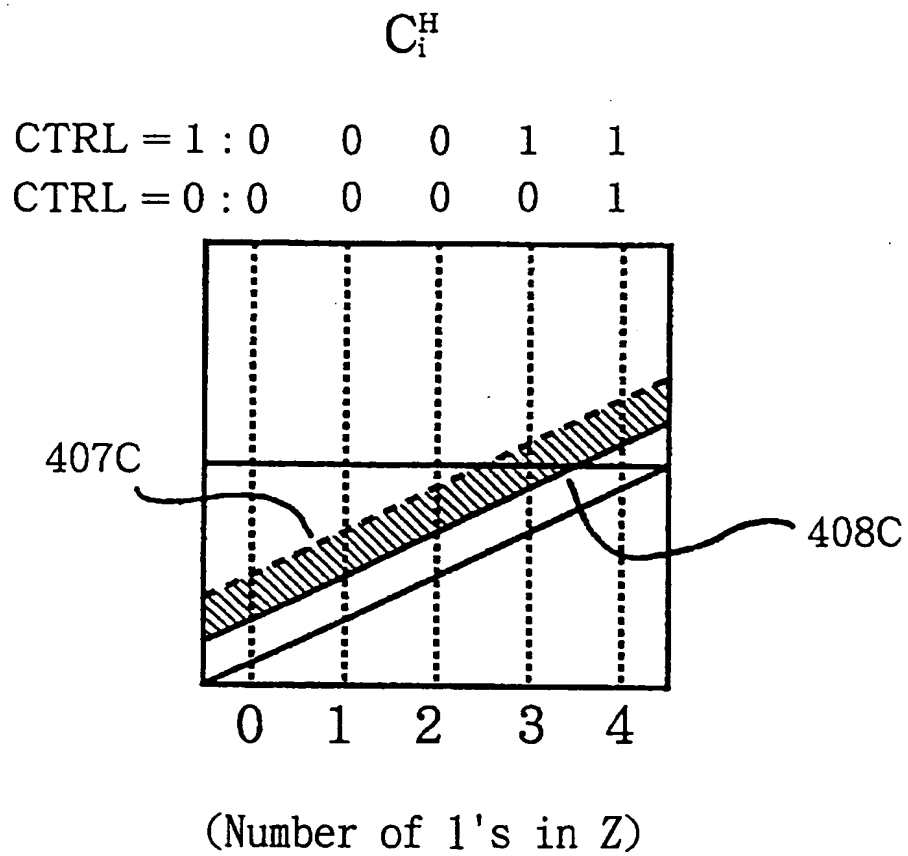


Fig. 11

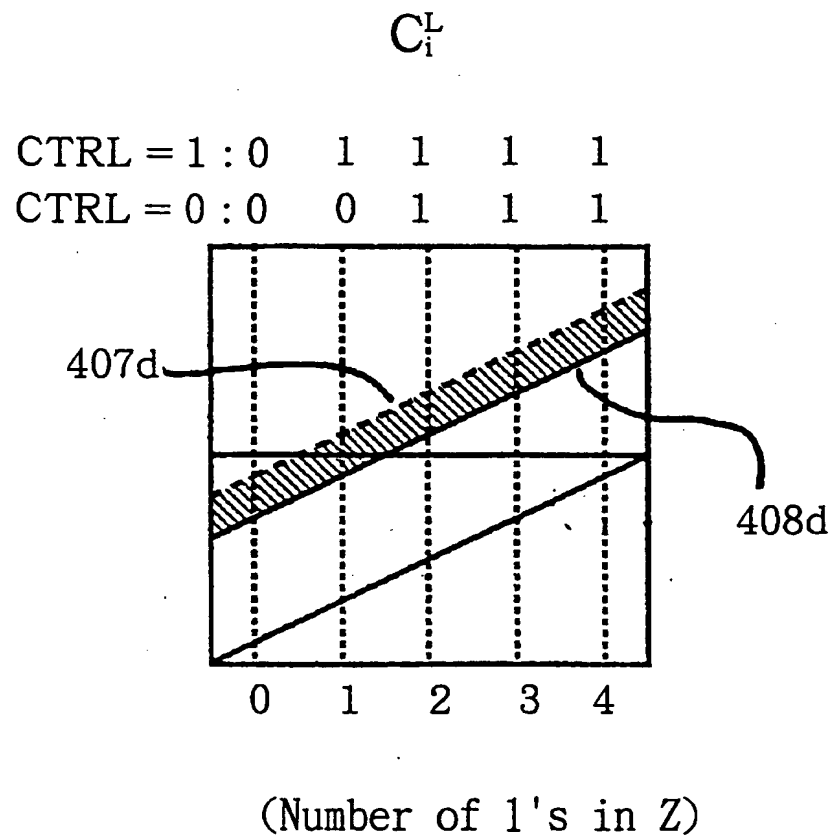


Fig. 12

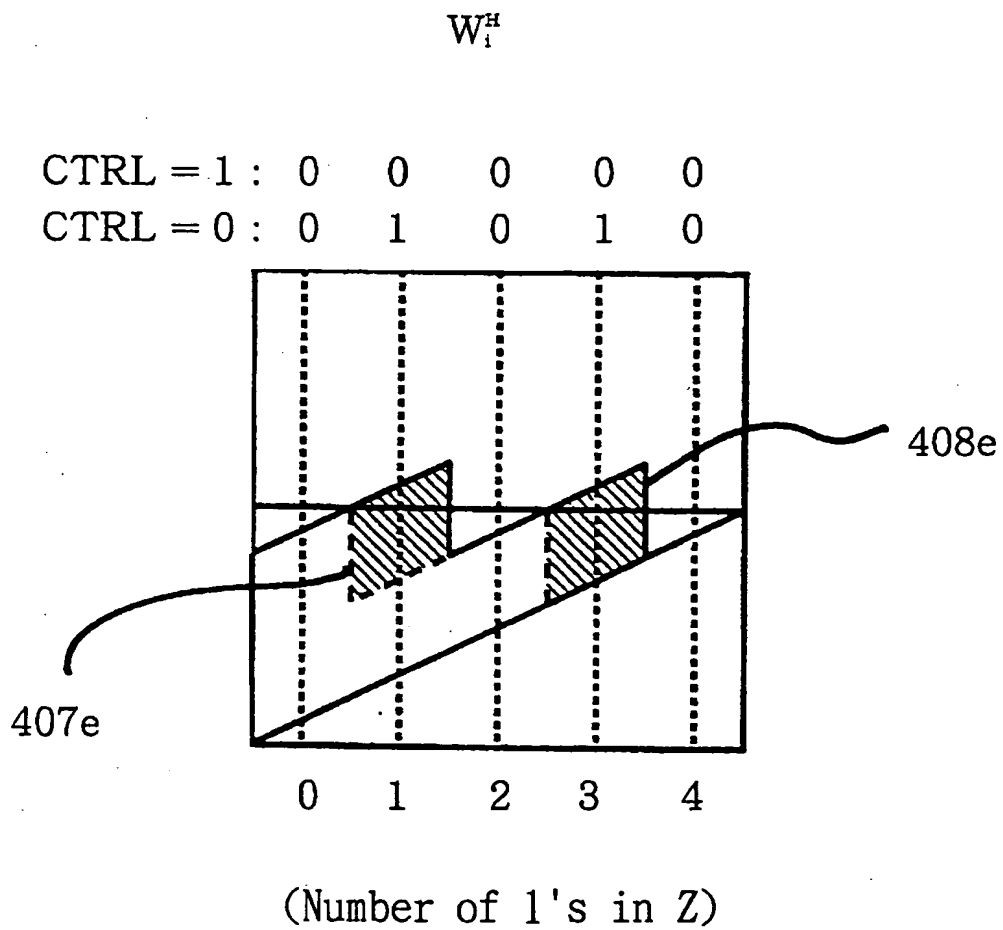


Fig. 13

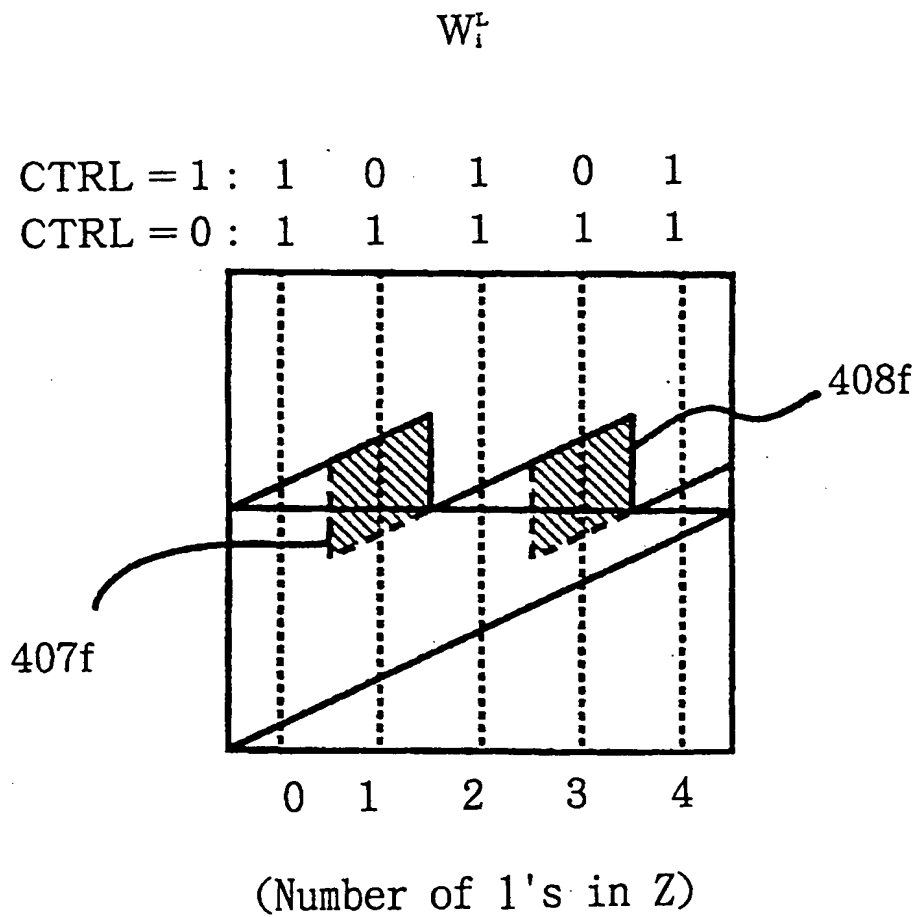


Fig. 14

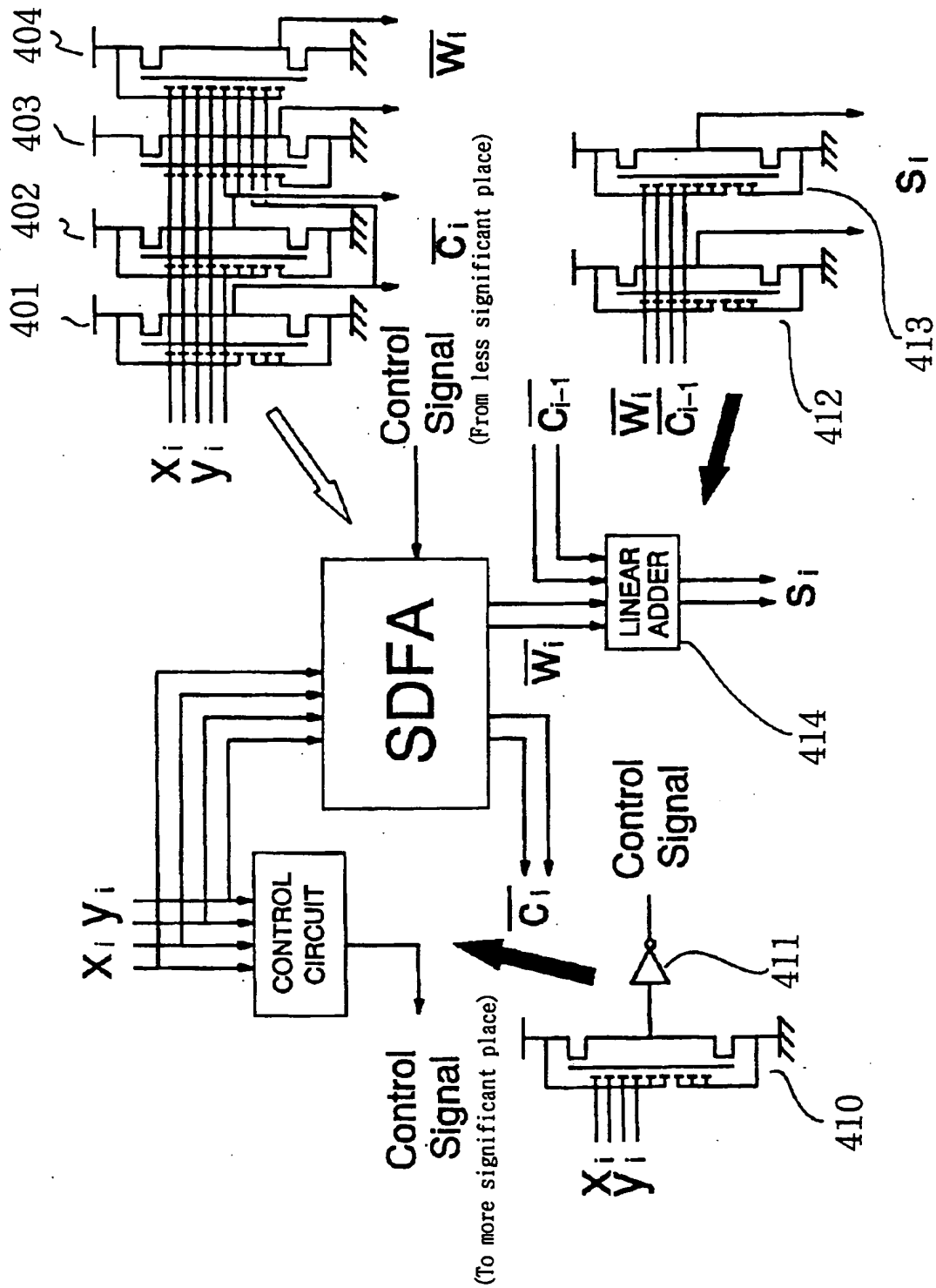


Fig. 15

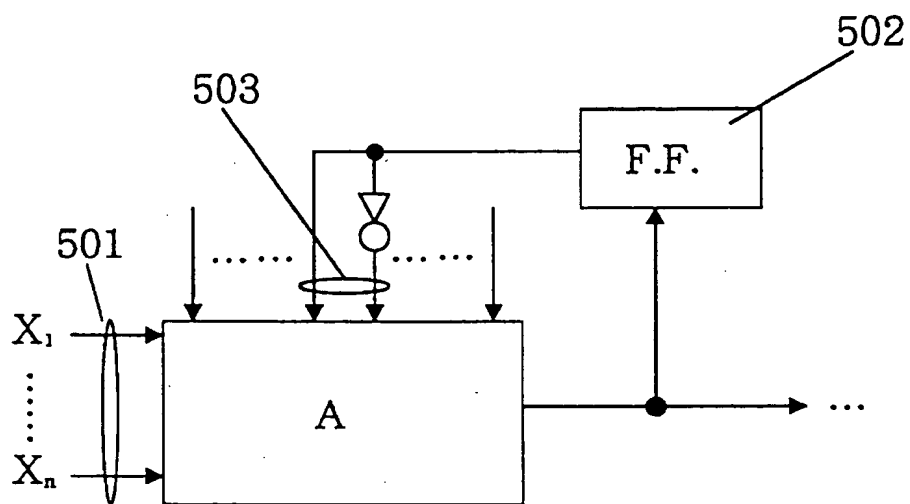


Fig. 16

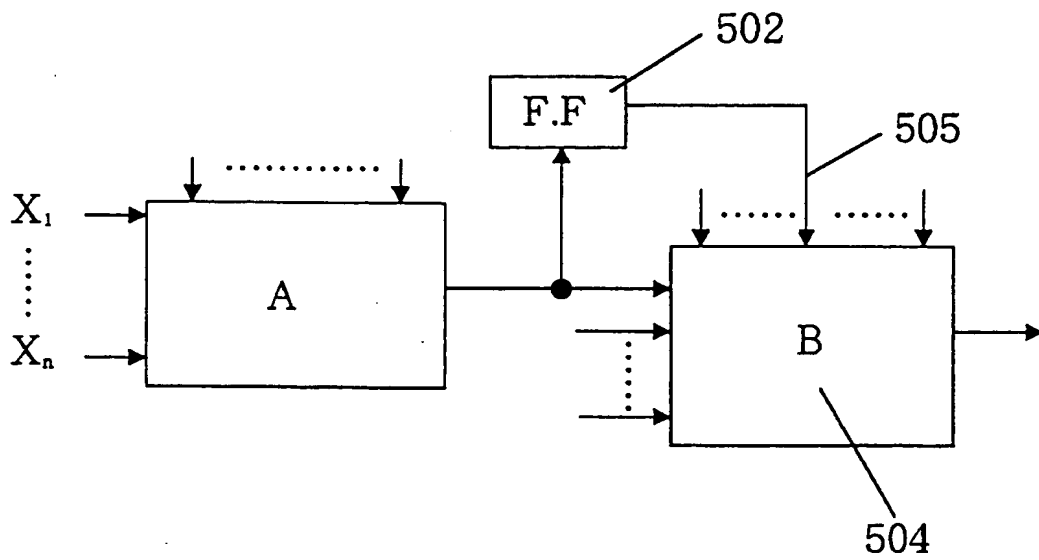


Fig. 17

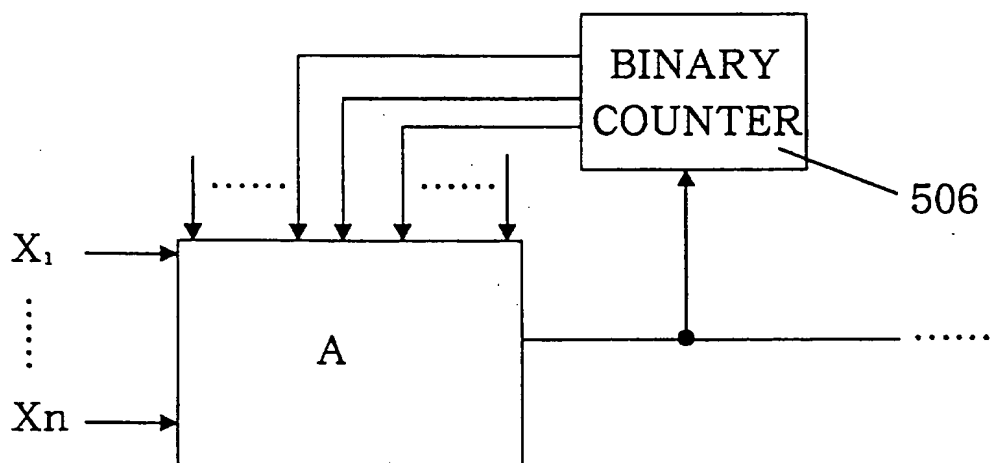
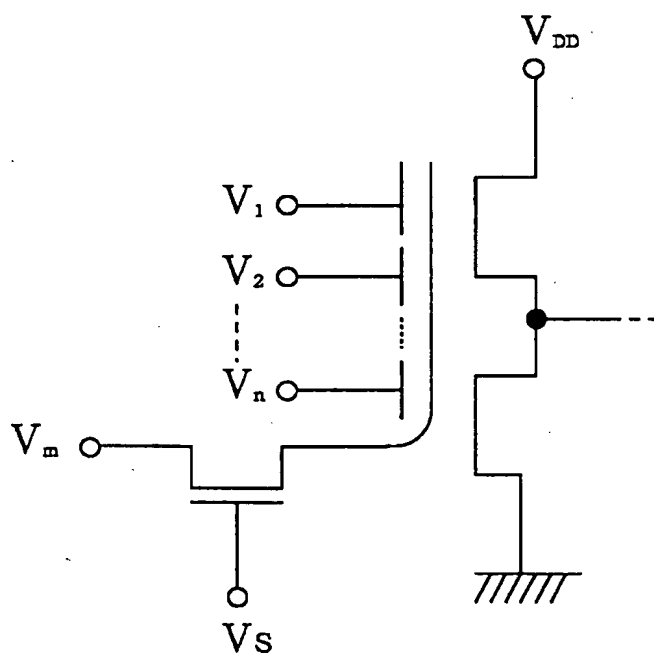


Fig. 18



# INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP94/00264

## A. CLASSIFICATION OF SUBJECT MATTER

Int. Cl<sup>5</sup> G06G7/60

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int. Cl<sup>5</sup> G06G7/60, G06F15/18

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Jitsuyo Shinan Koho 1975 - 1994

Kokai Jitsuyo Shinan Koho 1974 - 1994

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP, A, 4-71063 (Fujitsu Ltd.), March 5, 1992 (05. 03. 92), (Family: none)	1, 2

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

\* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

June 17, 1994 (17. 06. 94)

Date of mailing of the international search report

July 19, 1994 (19. 07. 94)

Name and mailing address of the ISA/

Japanese Patent Office

Authorized officer

Facsimile No.

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